

Turis Schematic STR (FT4)

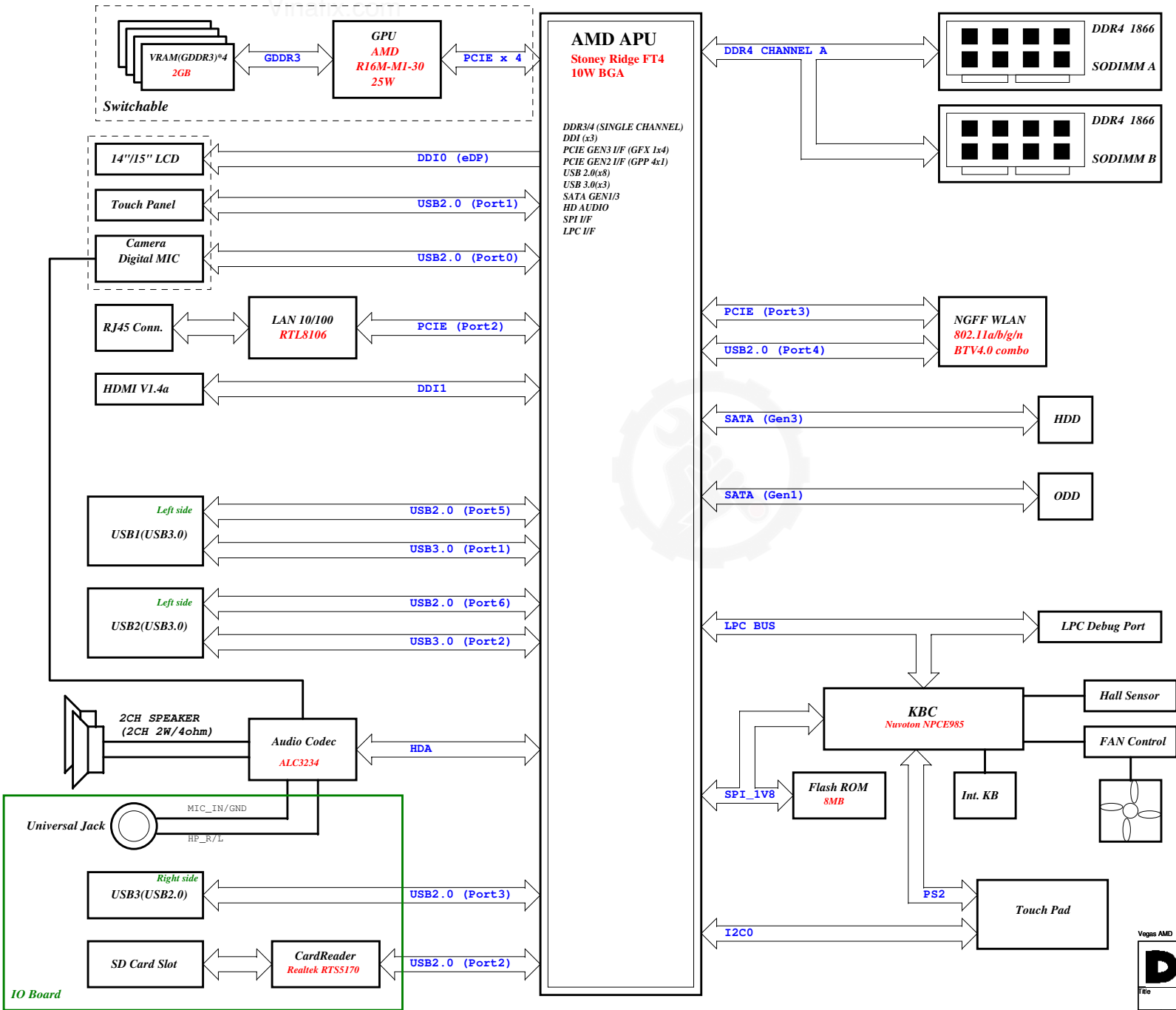
2016-08-30
REV : A00

DY : None Installed
UMA: UMA only installed
PX: DISCRTE PowerExpress installed

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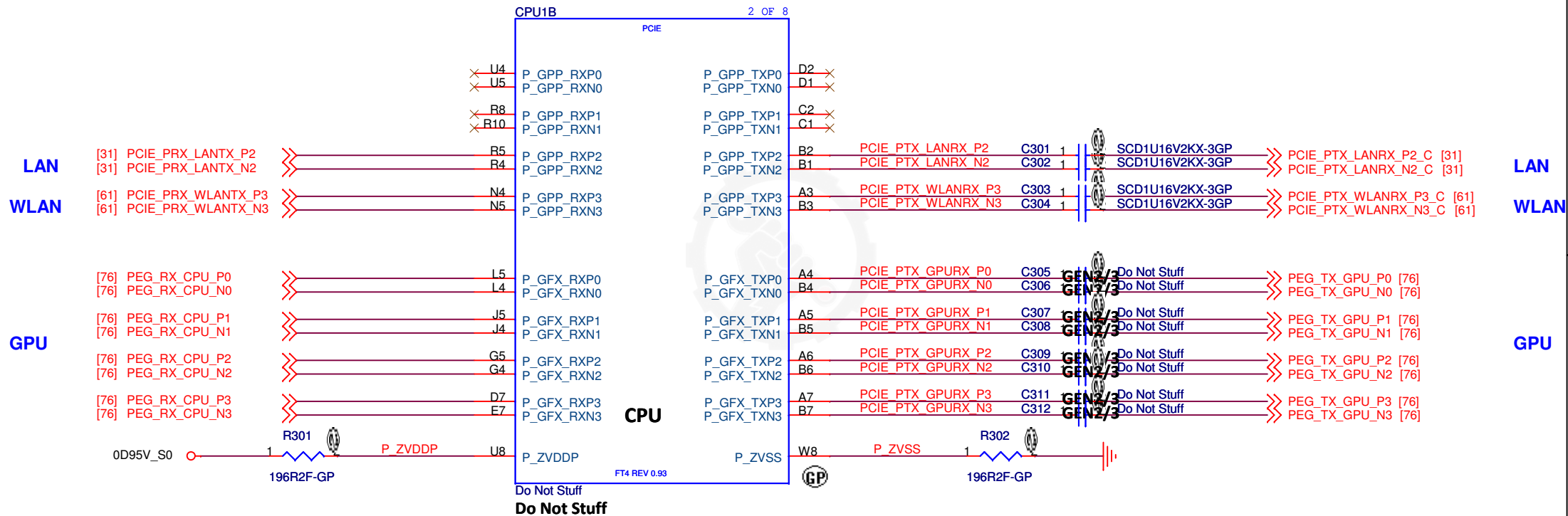
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Title			
Cover Page			
Size A3	Document Number		Rev A00
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Turis Stoney Ridge (FT4) Block Diagram



CHARGER		44
ISL88739HRZ-T		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
TPS51225RUKR		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core Power		46, 47
ISL62771HRTZ		
INPUTS	OUTPUTS	
DCBATOUT	1V_CPU_CORE 1D2V_CPU_VDDNB	
DDR4 SUS		53
APW8861QBI-TRG		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3 0D6V_VREF_S0	
CPU VDDP		52
APW8861QBI-TRG		
INPUTS	OUTPUTS	
DCBATOUT	0D95V_S5	
CPU VDD18		54
RT8068AZQWID		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
CPU VDDCRGFX		49
APL5337KAI		
INPUTS	OUTPUTS	
1D8V_S5	0D775V_S5	
Switches		40
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
1D8V_S5	1D8V_S0	
0D95V_S5	0D95V_S0	
PCB LAYER		
L1: TOP L2: VCC L3: Signal L4: Signal L5: GND L6: BOT		

GPP CLK port	Device	CLKREQ#
2	LAN	2
3	WLAN	3
G	GPU	G



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CPU (PCIE)Size
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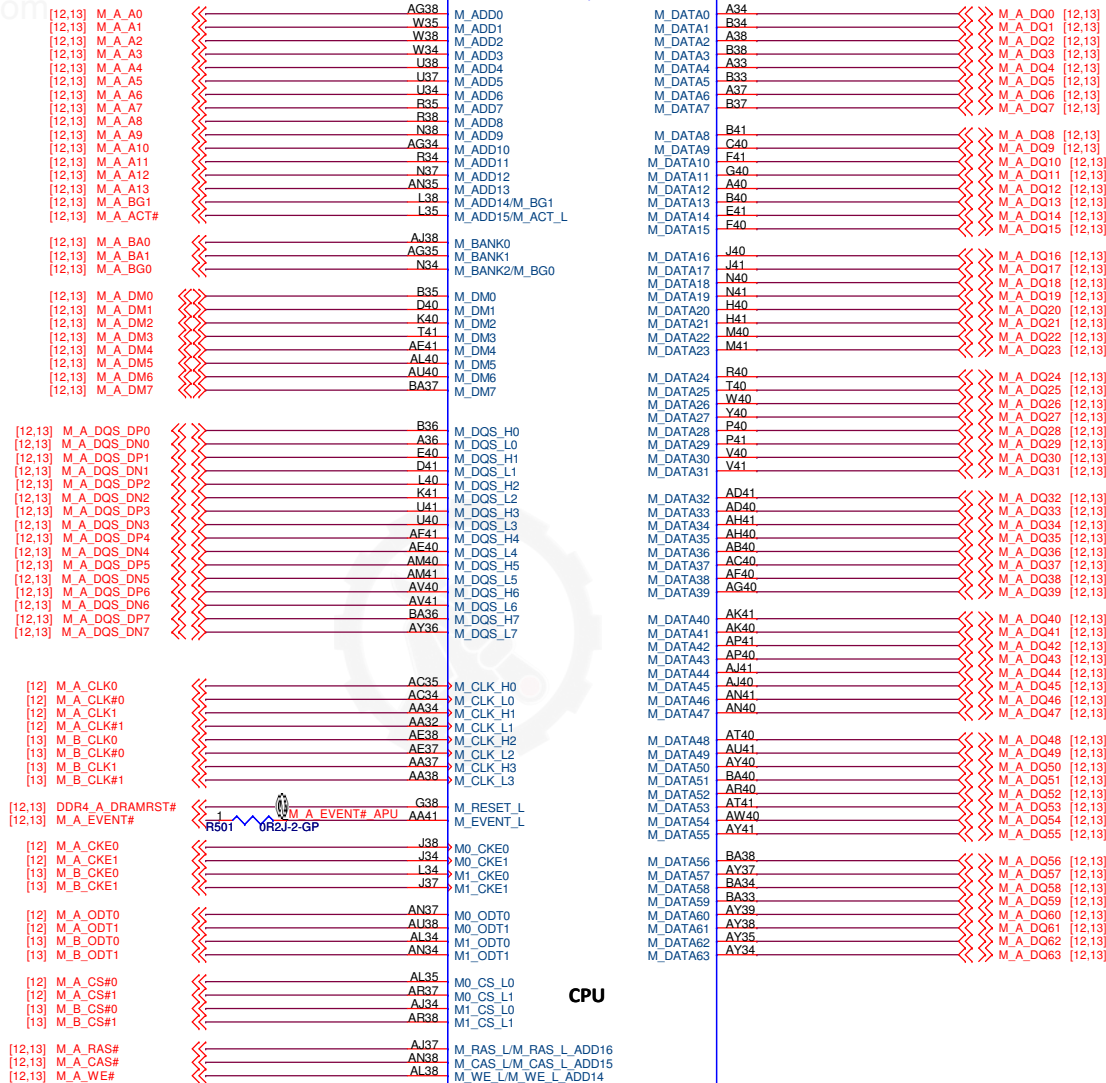
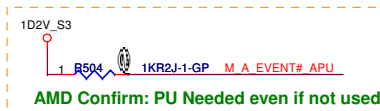
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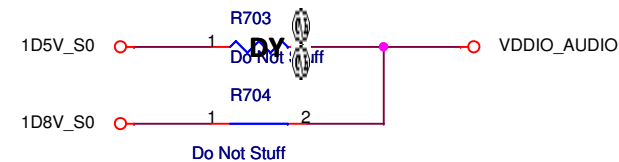
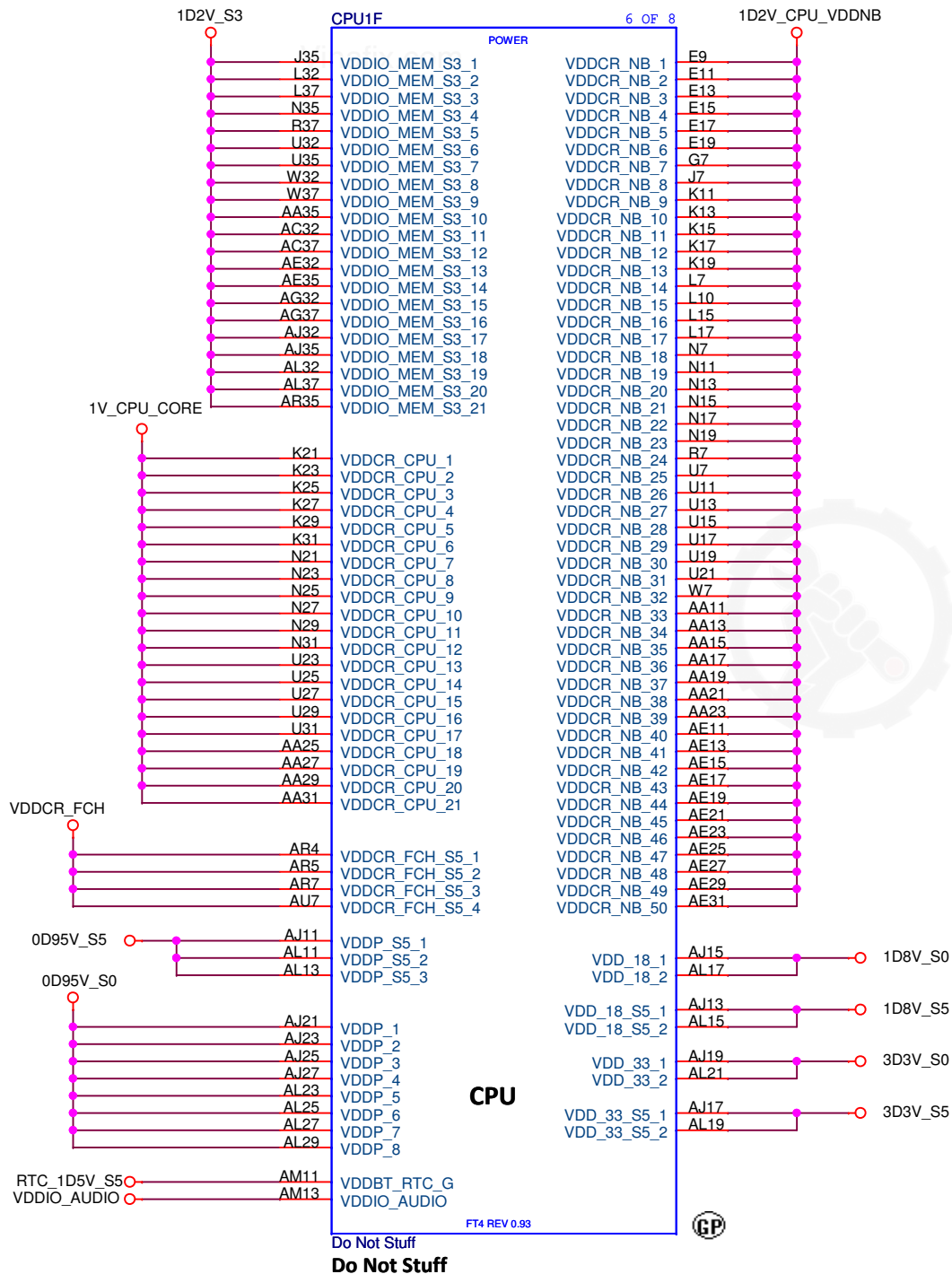
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Title

CPU(VCC CORE)

Size
A4

Document Number

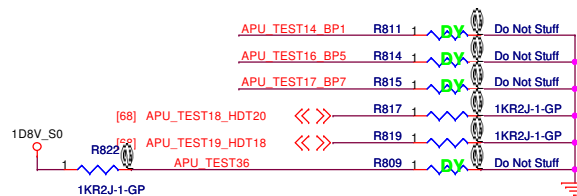
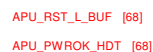
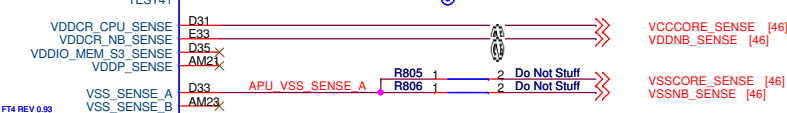
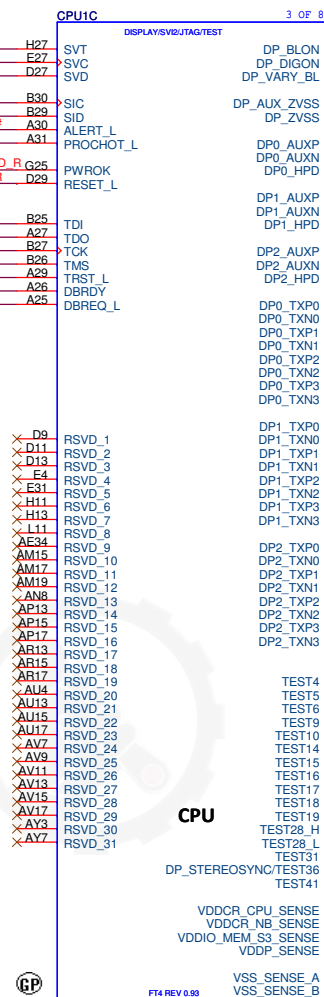
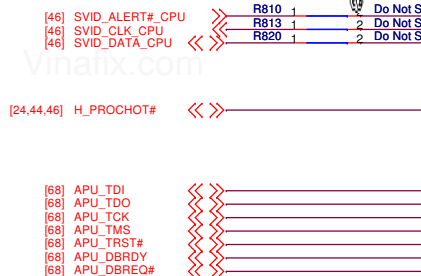
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SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



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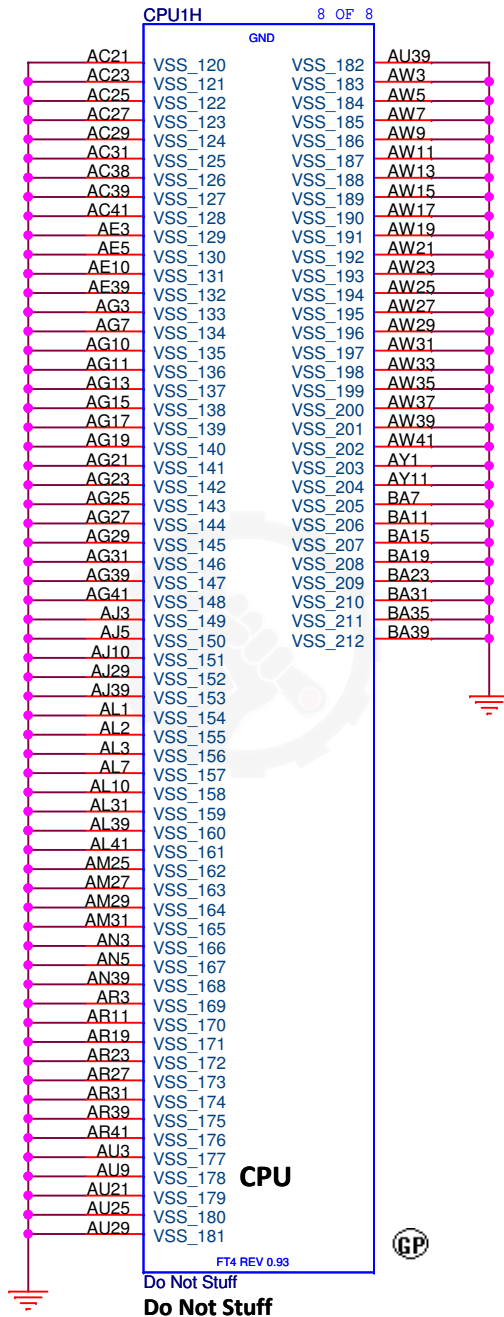
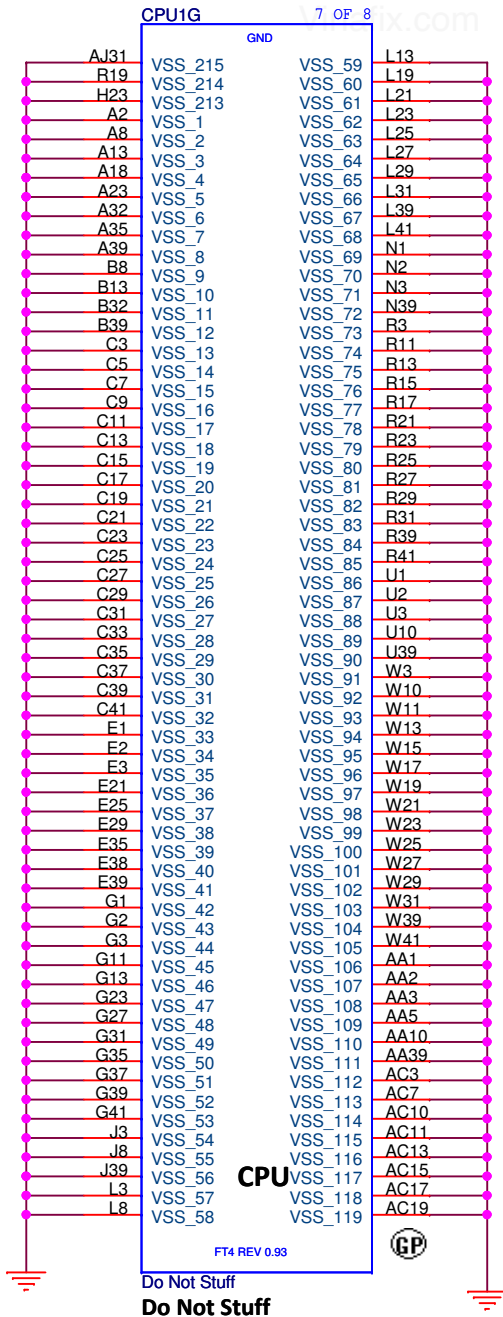


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Title	CPU (DISPLAY/SVI2/JTAG/TES)
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Title

CPU (VSS)

Size
A4

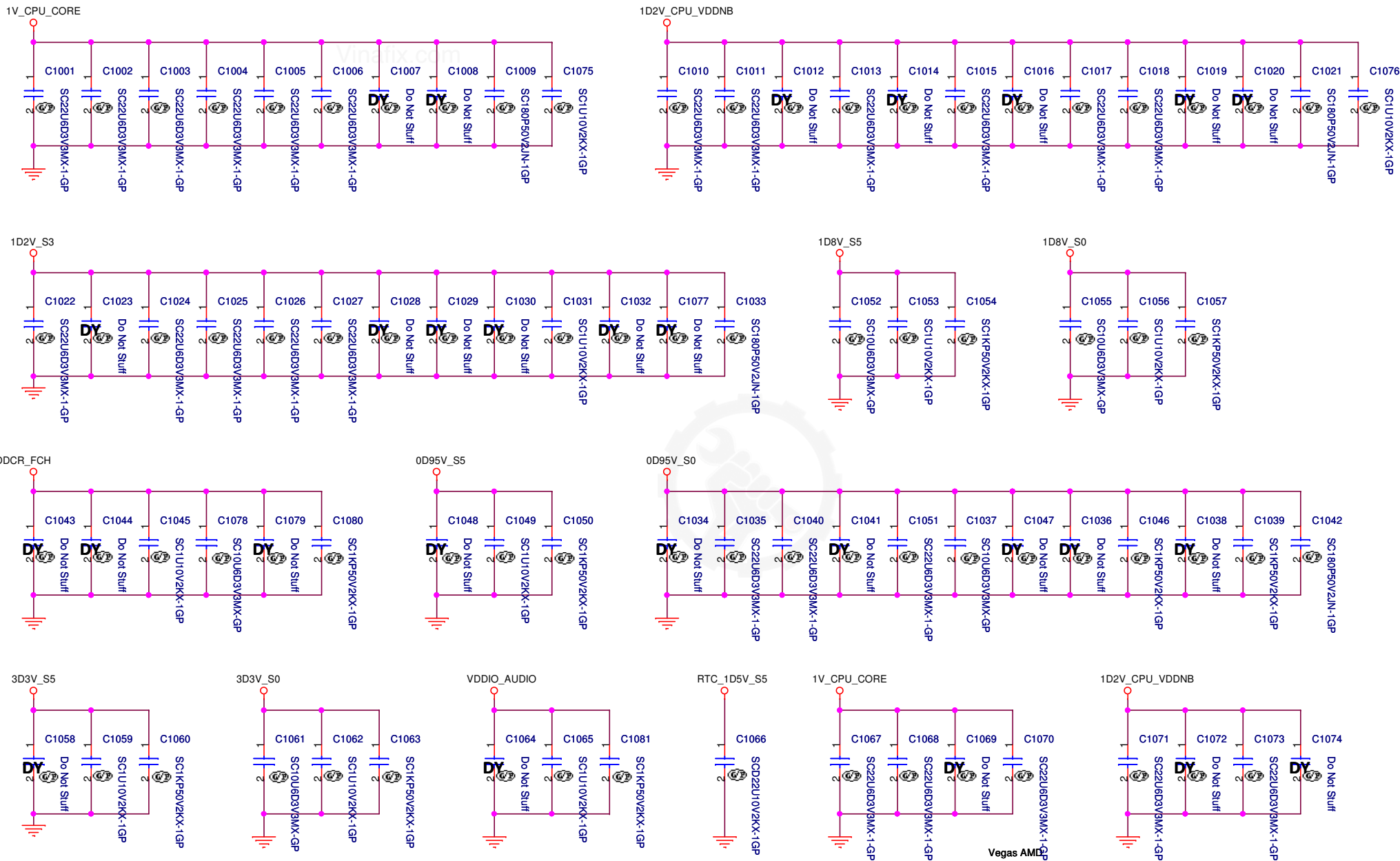
Document Number

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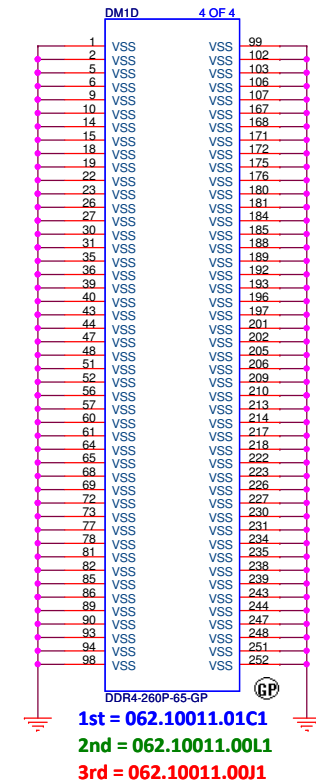
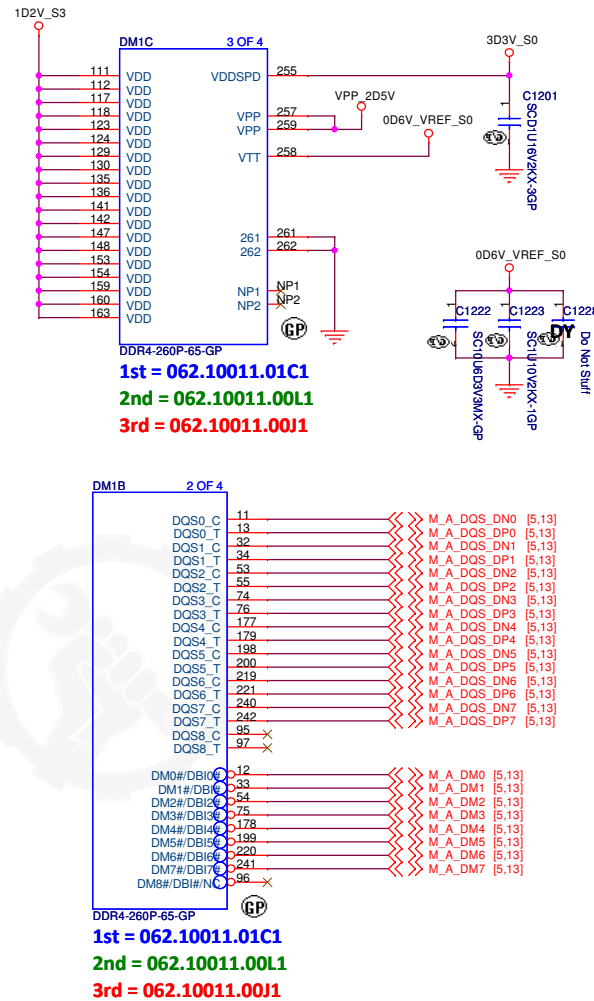
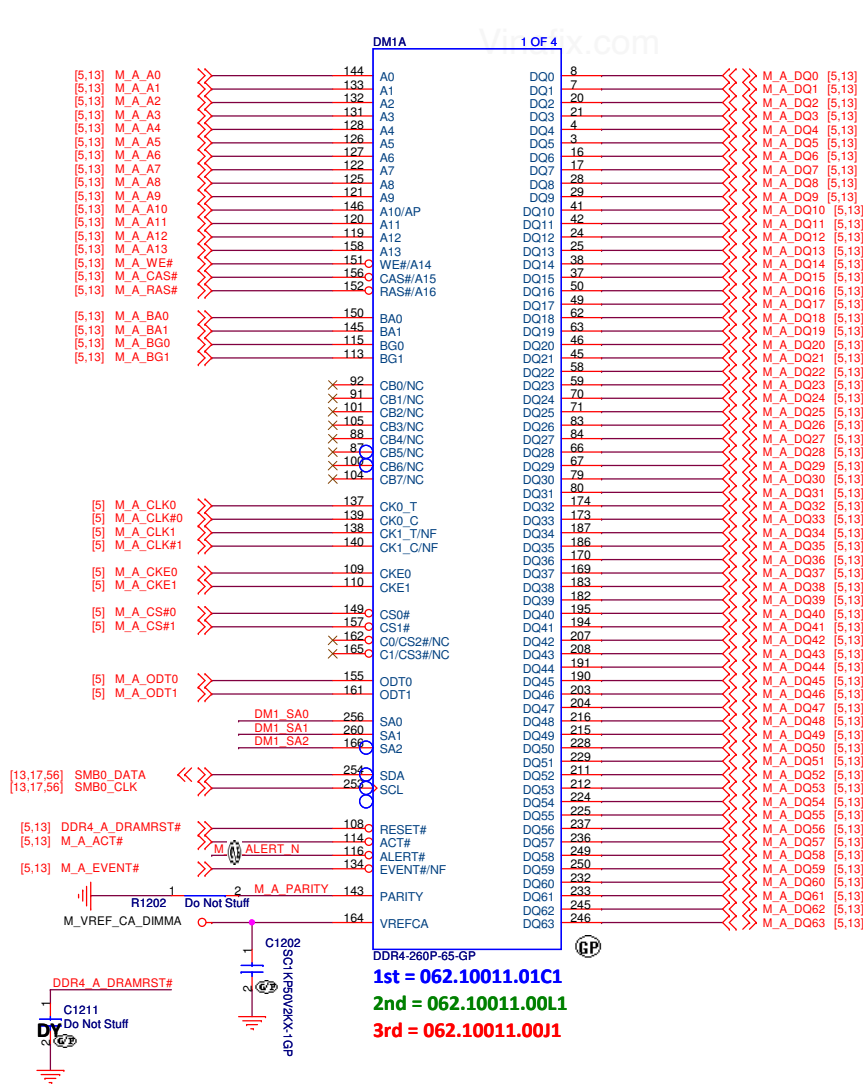
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CPU (Power CAP1)					
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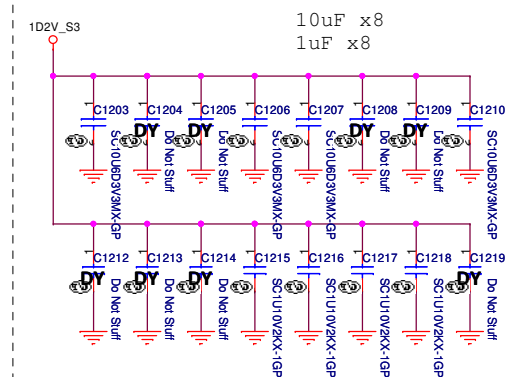
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SSID = DDR4-SODIMM1



```
| Layout Note :  
| Place these Caps near DIM1
```



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Title

DDR4-SODIMM1Size
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Document Number	
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Rev	
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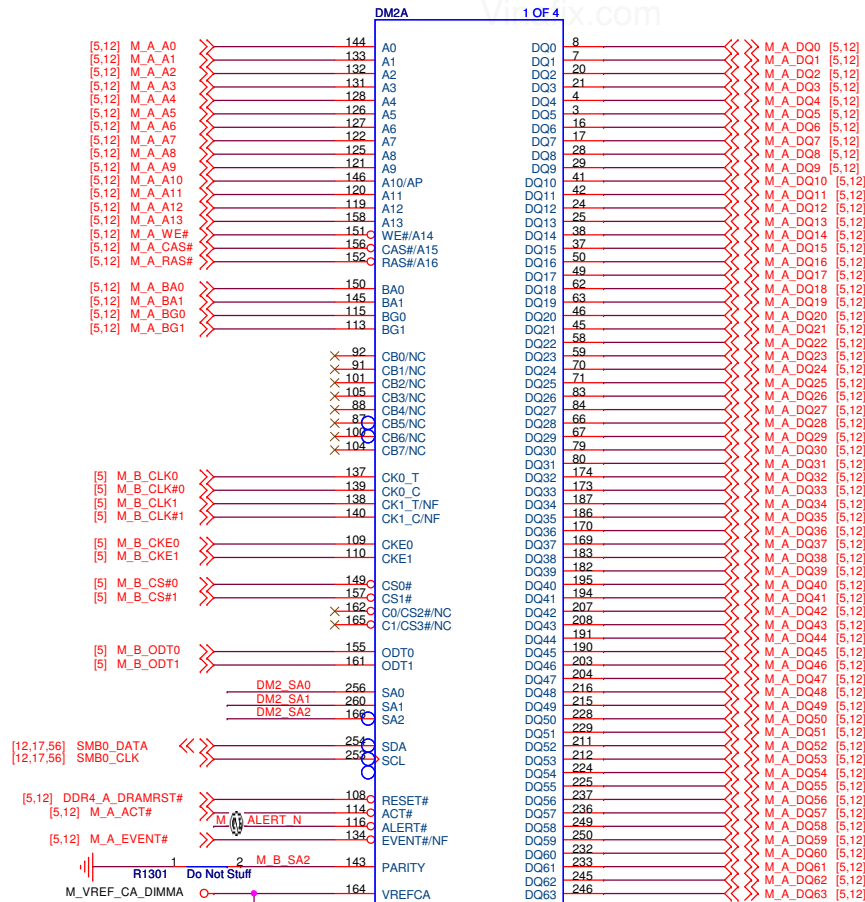
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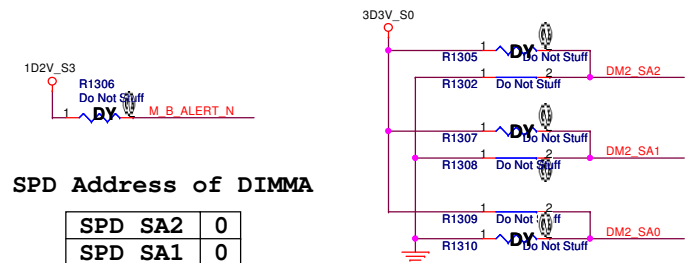
SPD Address of DIMMA

SPD SA2	0
SPD SA1	0
SPD SA0	0

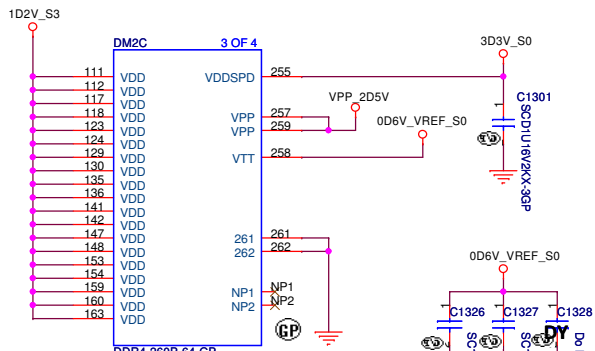
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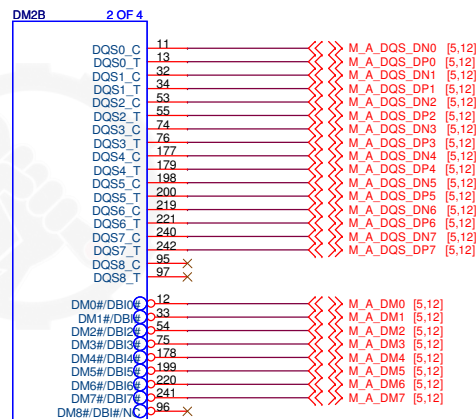
DDR4-260P-64-GP
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2nd = 062.10011.00R1
3rd = 062.10011.00K1
4th = 062.10011.00I1



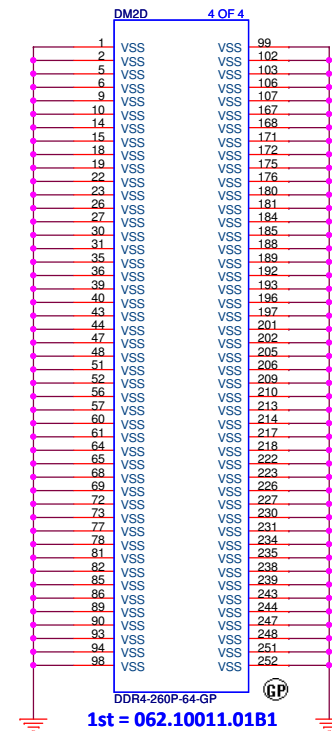
SPD SA2	0
SPD SA1	0
SPD SA0	1



DDR4-260P-64-GP
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2nd = 062.10011.00R1
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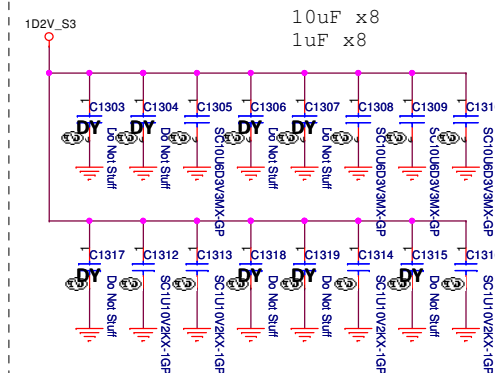


DDR4-260P-64-GP
1st = 062.10011.01B1
2nd = 062.10011.00R1
3rd = 062.10011.00K1
4th = 062.10011.00I1



DDR4-260P-64-GP
1st = 062.10011.01B1
2nd = 062.10011.00R1
3rd = 062.10011.00K1
4th = 062.10011.00I1

Layout Note :
 Place these Caps near DIM1



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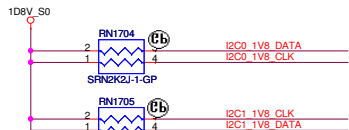
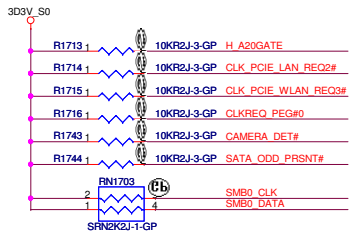
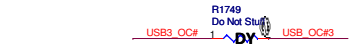
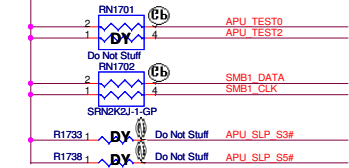
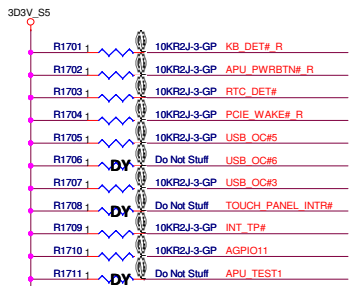
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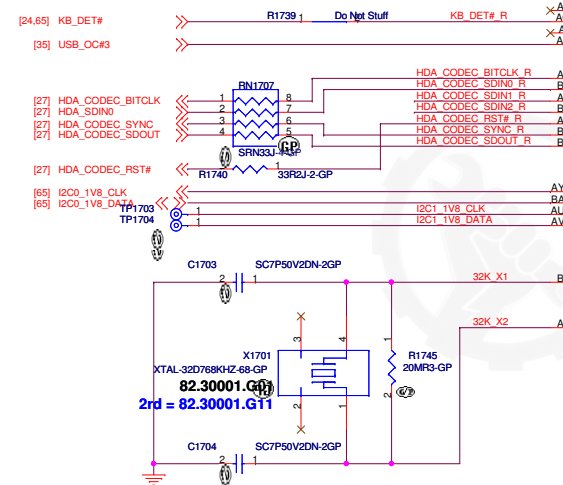
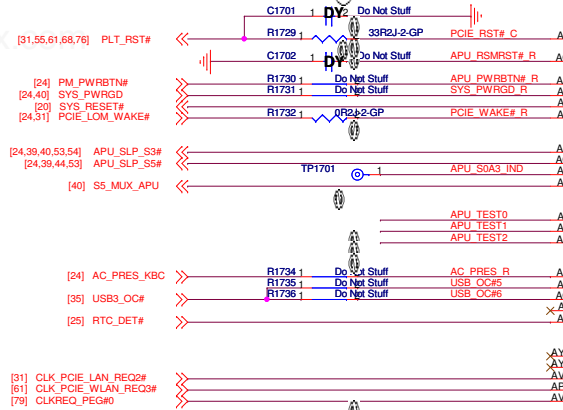
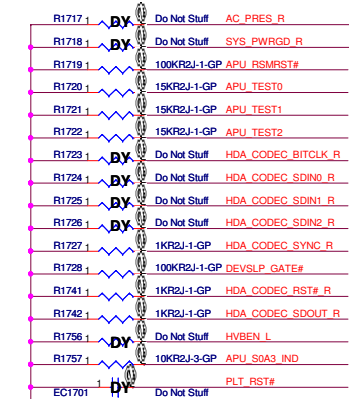
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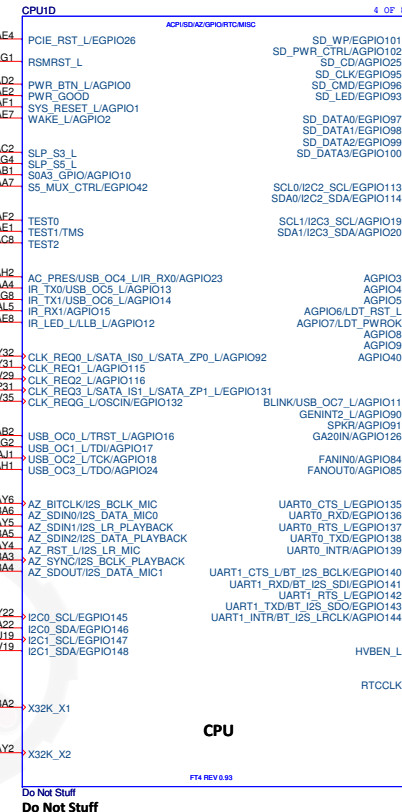
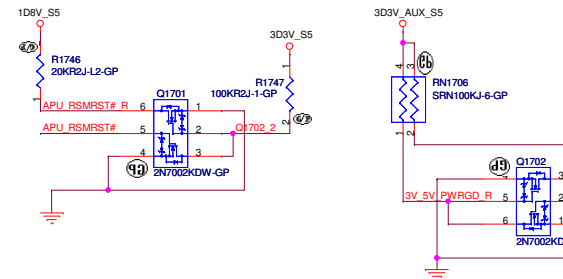
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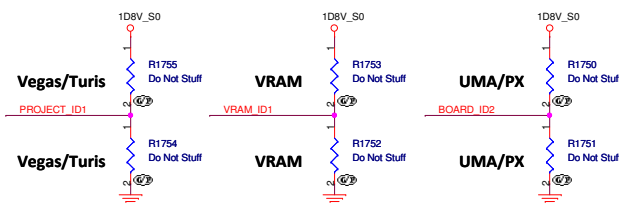
Pull-up 10Kohm if not used.



Crystal ESR should be between 10Kohm to 65Kohm.



	1	0
BOARD_ID2	UMA	DIS
PROJECT_ID1	Vegas	Turis
VRAM_ID1	2GB	4GB



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Title **CPU(ACPI/SD/AZ/GPIO/RTC)**

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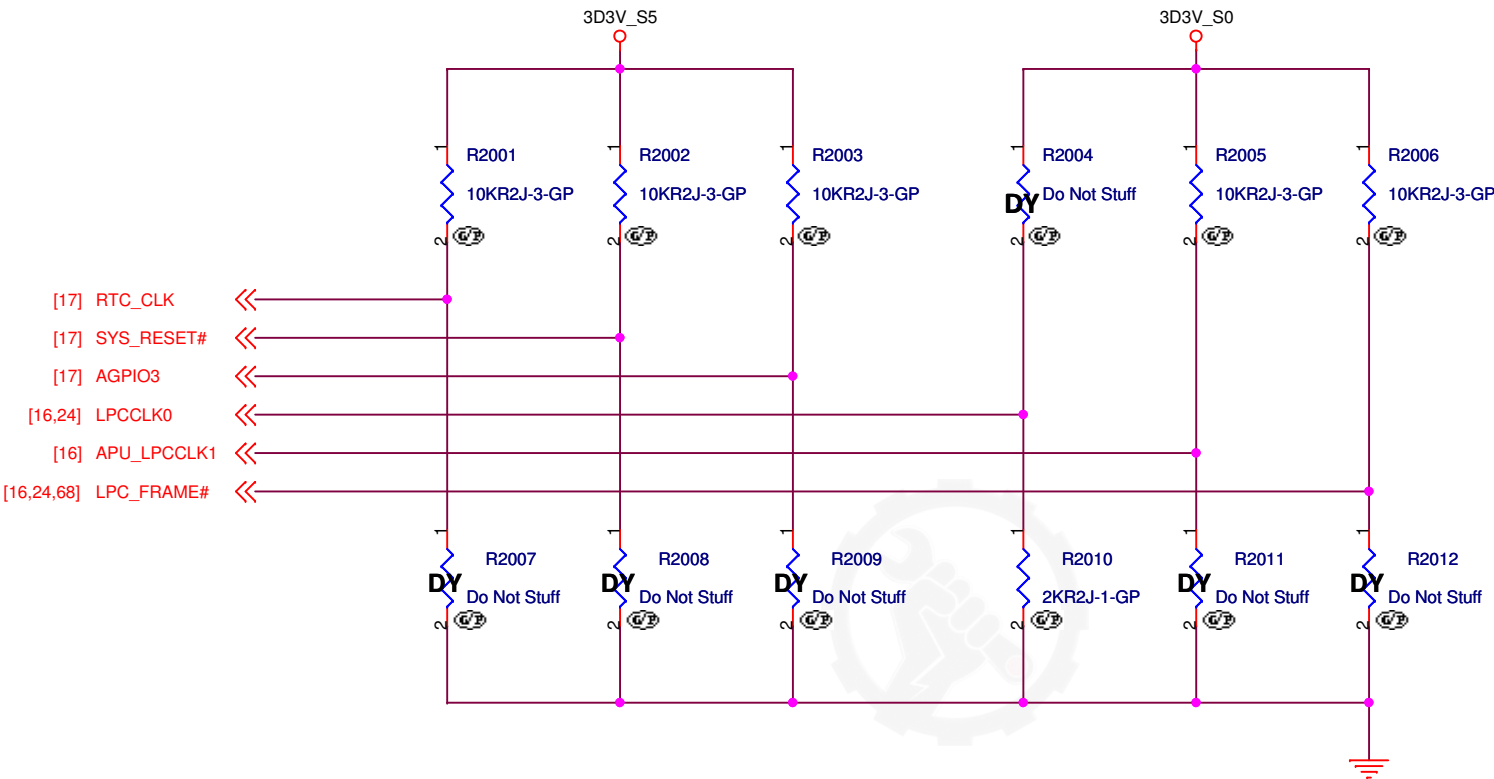
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SYSTEM STRAPPINGS



REQUIRED SYSTEM STRAPS

	RTC_CLK	SYS_RESET#	AGPIO3	LPC_CLK0	LPC_CLK1	LPC_FRAME#
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

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CPU Strappings

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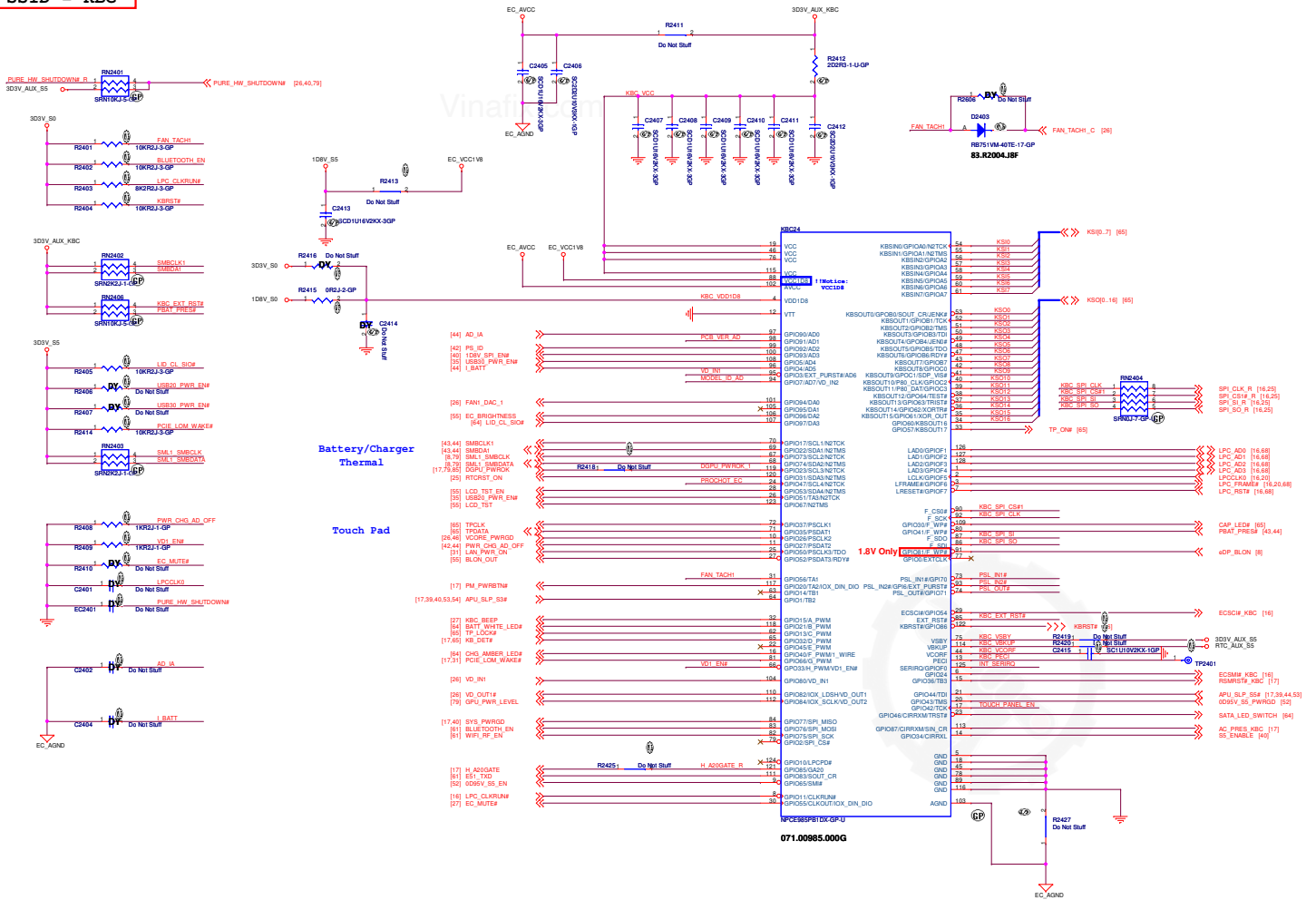
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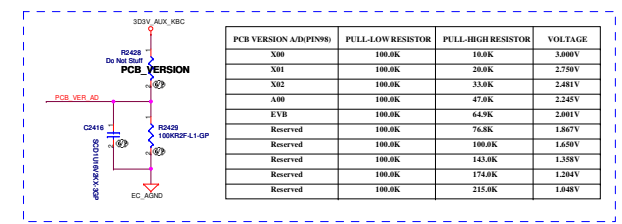
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SSID = KBC



PCB Version

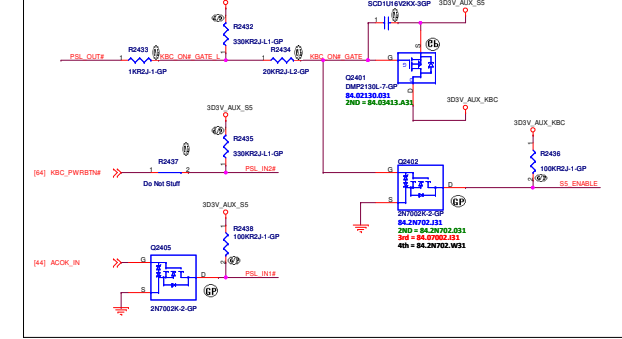


PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.000V
X01	100.0K	20.0K	2.750V
X02	100.0K	33.0K	2.481V
A00	100.0K	47.0K	2.245V
EVB	100.0K	64.9K	2.091V
Reserved	100.0K	76.9K	1.967V
Reserved	100.0K	100.0K	1.850V
Reserved	100.0K	143.0K	1.735V
Reserved	100.0K	174.0K	1.624V
Reserved	100.0K	215.0K	1.548V

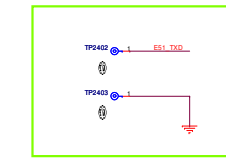
R2453 for SKU Control

MODEL_ID_DET(GPIO7)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
T000	100.0K	10.0K (64.10023.400.1)	3.00V
T001	100.0K	20.0K (64.10023.400.1)	2.75V
T002	100.0K	33.0K (64.10023.400.1)	2.48V
T003	100.0K	47.0K (64.10023.400.1)	2.25V
T004	100.0K	64.9K (64.10023.400.1)	2.09V
T005	100.0K	76.9K (64.10023.400.1)	1.97V
T006	100.0K	100.0K (64.10023.400.1)	1.85V
T007	100.0K	143.0K (64.10023.400.1)	1.73V
T008	100.0K	174.0K (64.10023.400.1)	1.62V
T009	100.0K	215.0K (64.10023.400.1)	1.55V

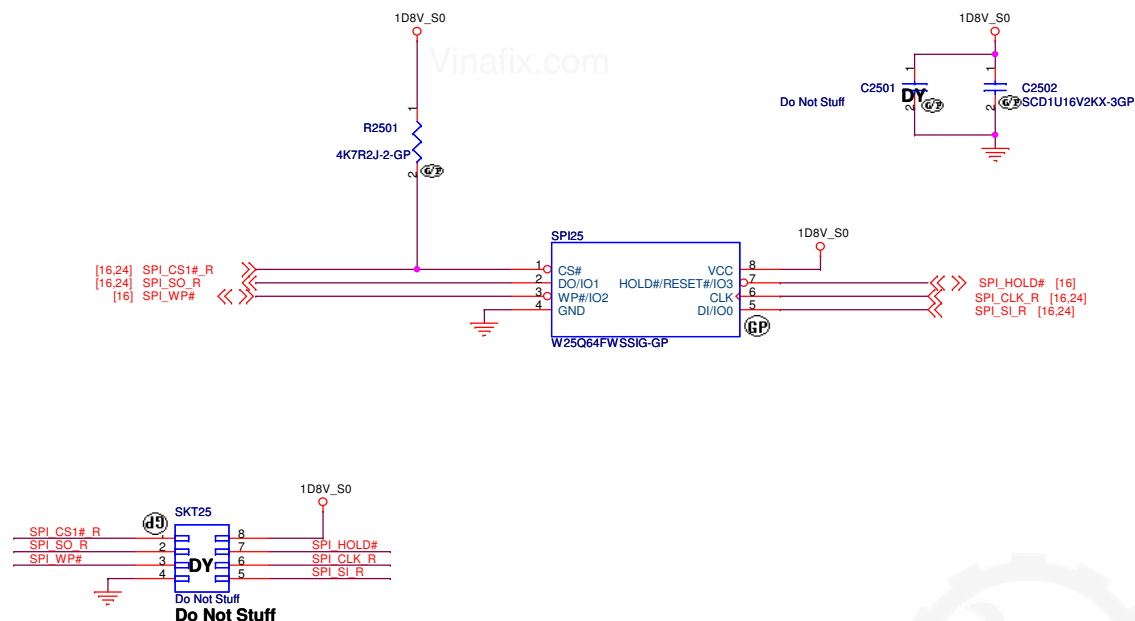
Start up



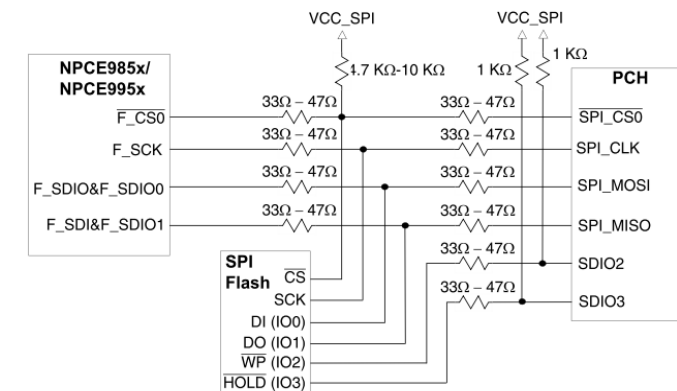
Layout Note: Place it on Bottom Side.



SSID = Flash.ROM

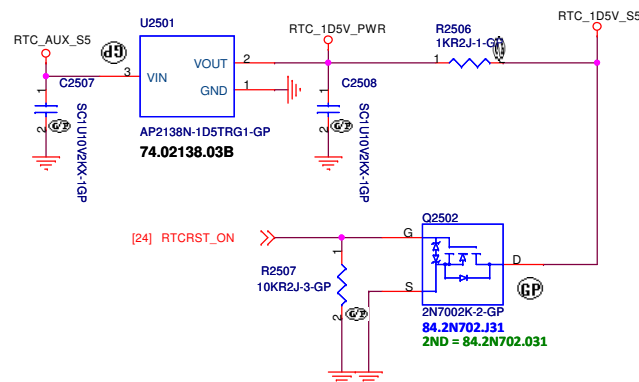
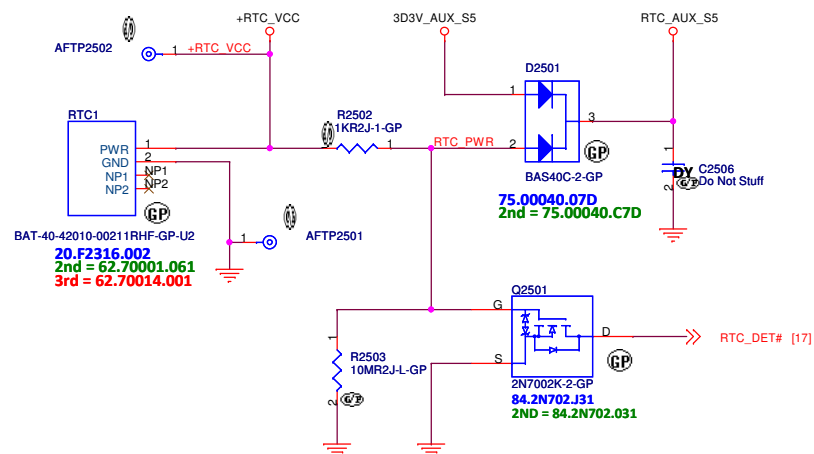


Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RTC

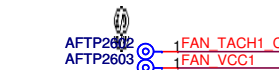
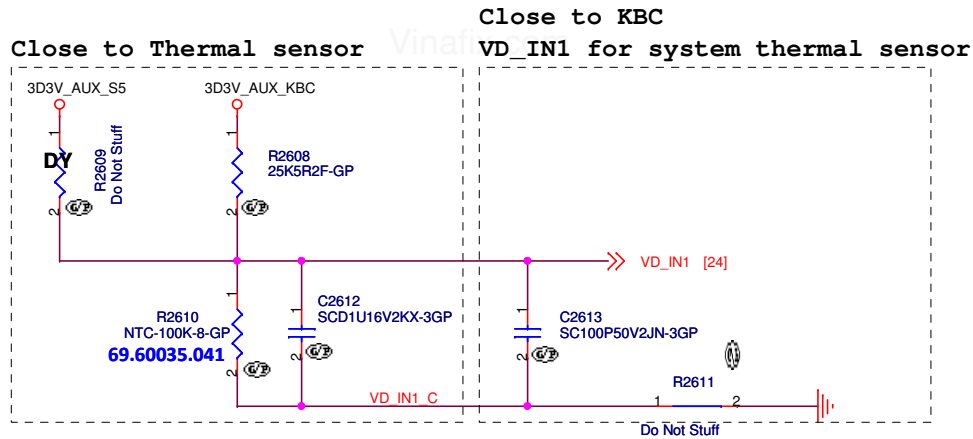


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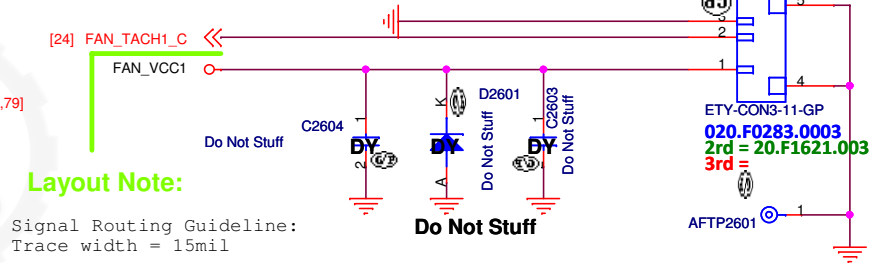
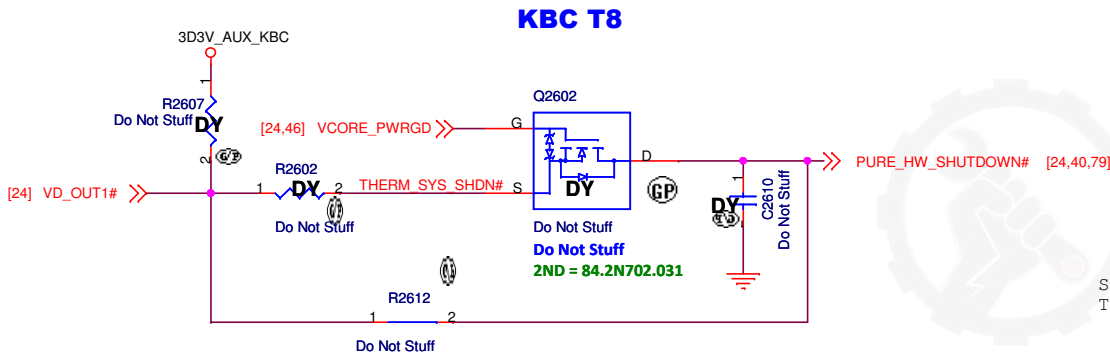
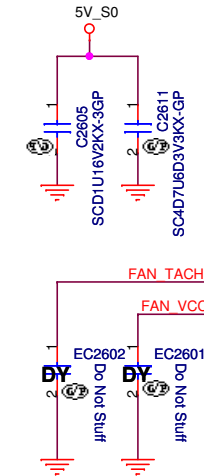
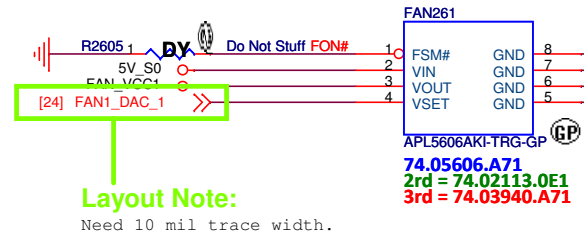
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash ROM/RTC**
Size: A3 Document Number: **Turis STR (FT4)** Rev: **A00**
Date: Monday, August 29, 2016 Sheet 25 of 106

SSID = Thermal



Fan controller1

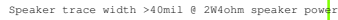


Vegas AMD

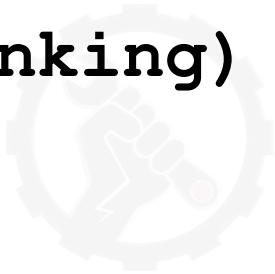
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title THERMAL W/Fan			
Size Custom	Document Number Turis STR (FT4)		Rev A00
Date: Monday, August 29, 2016		Sheet 26 of 106	

	ALC3234	ALC3246
R2726	mount	DY
R2723	mount	DY
R1740	mount	DY
R2713	DY	DY
R2710	mount	mount
R2705	DY	mount
R2718	DY	mount

Try to Use 1D8V on 3234.



(Blanking)



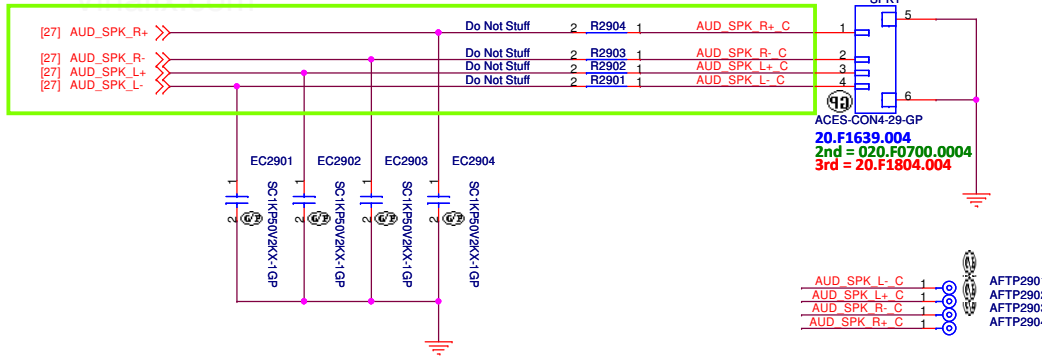
Vegas AMD

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Title (Reserved)			
Size A4	Document Number Turis STR (FT4)		Rev A00
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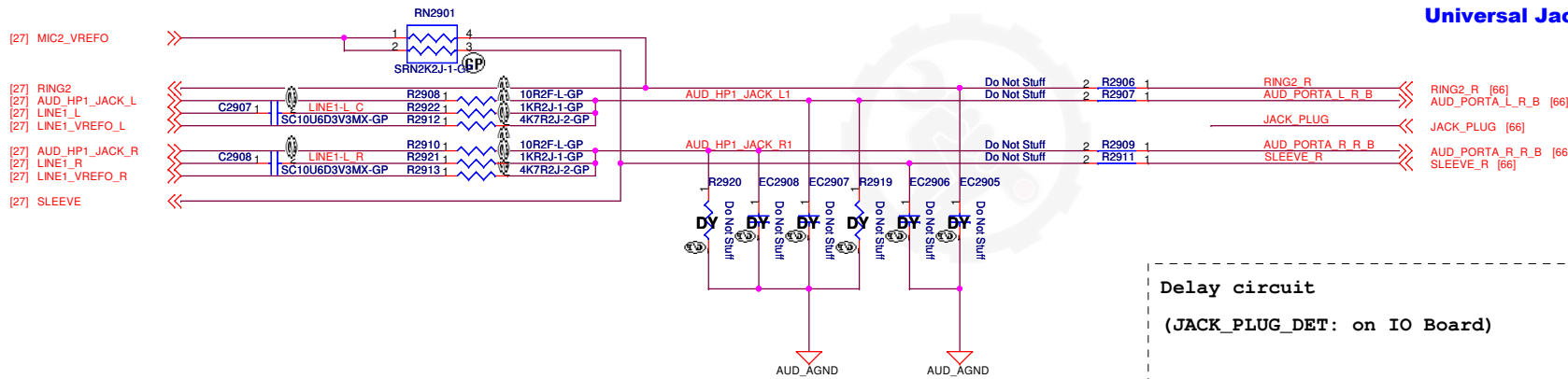
SSID = Speaker/Universal Jack

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



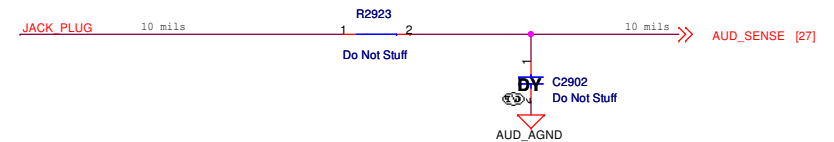
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Universal Jack (Moved to I/O Board)

Delay circuit

(JACK_PLUG_DET: on IO Board)



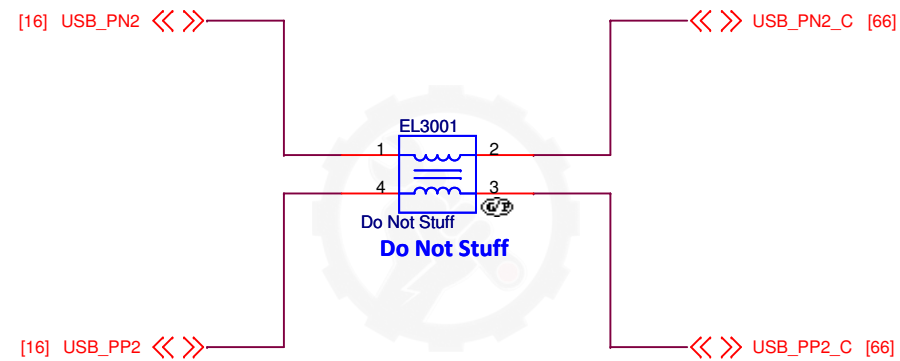
Vegas AMD

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Title		
Speaker/Universal Jack		
Size	Document Number	Rev
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Main Func = Card Reader

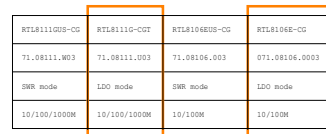
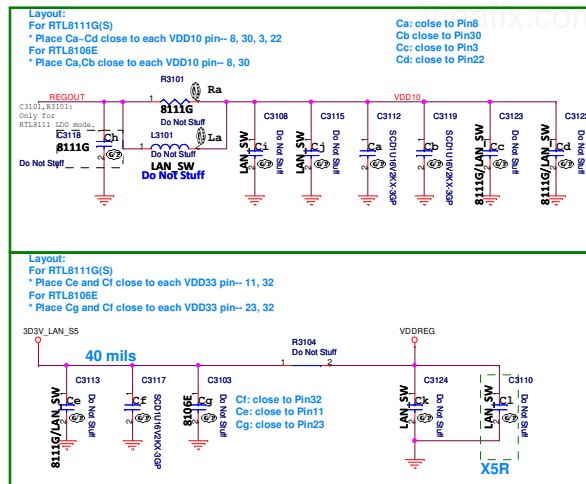
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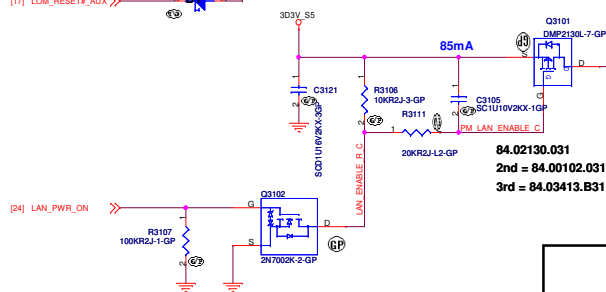
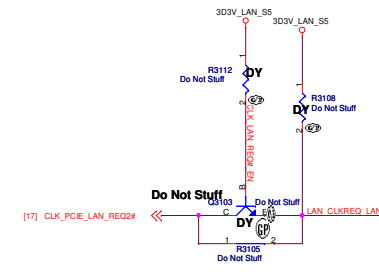
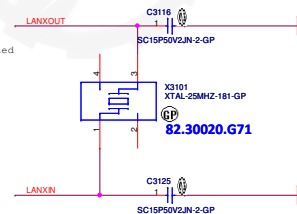
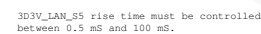
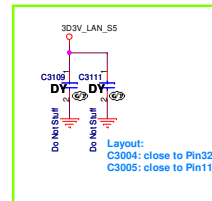
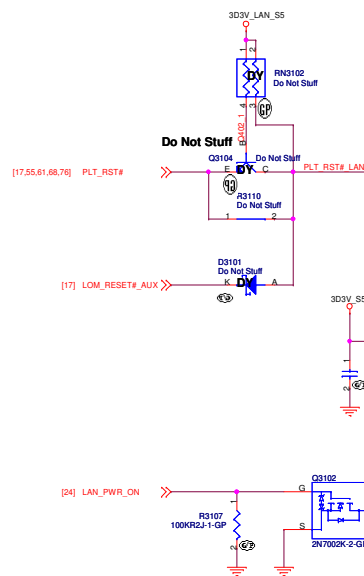
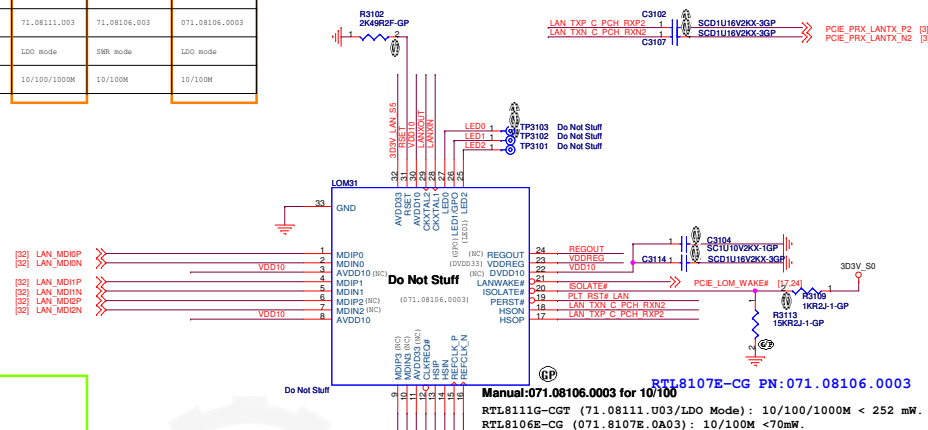
Vegas AMD

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Title Card Reader			
Size A4	Document Number Turis STR (FT4)		Rev A00
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```
SSID = LAN RTL8111/RTL8106
```

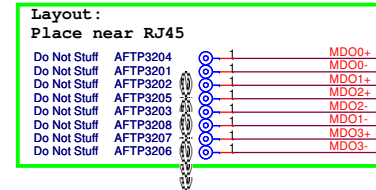
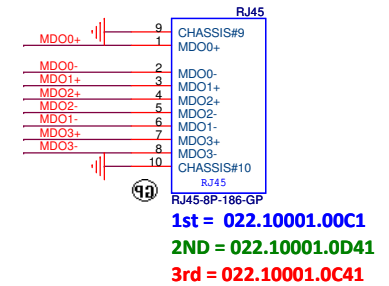
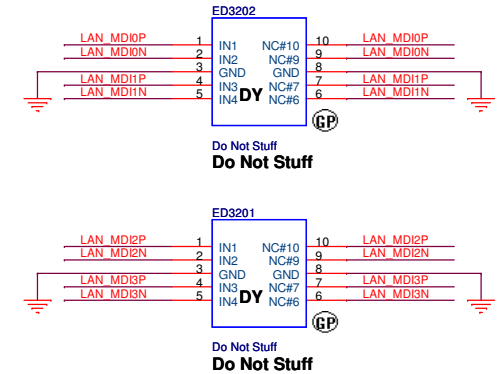
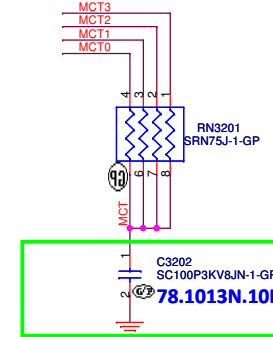
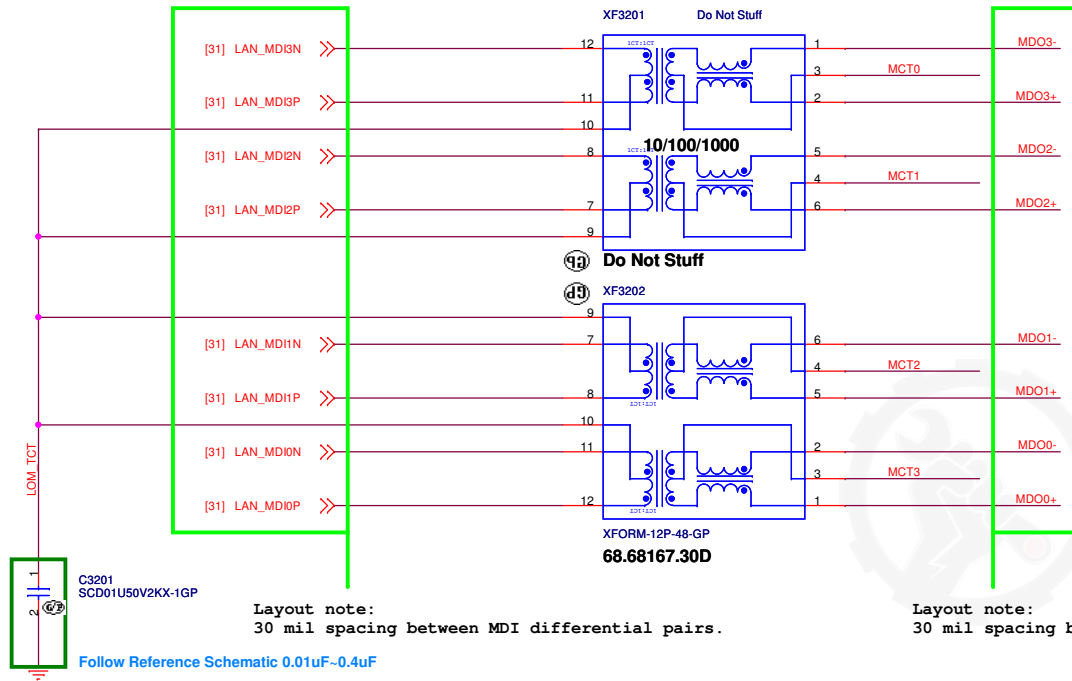


LAN CHIP (10/100/1000M & 10/100M co-lay)

[illegible]

SSID = LOM

LAN TransFormer (10/100/1000M & 10/100M co-lay)



(Blanking)

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Title (Reserved)			
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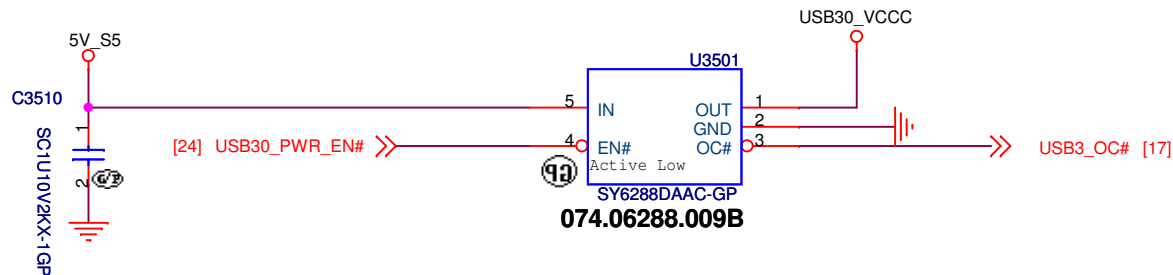
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Vegas AMD

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Title (Reserved)			
Size A4	Document Number Turis STR (FT4)		Rev A00
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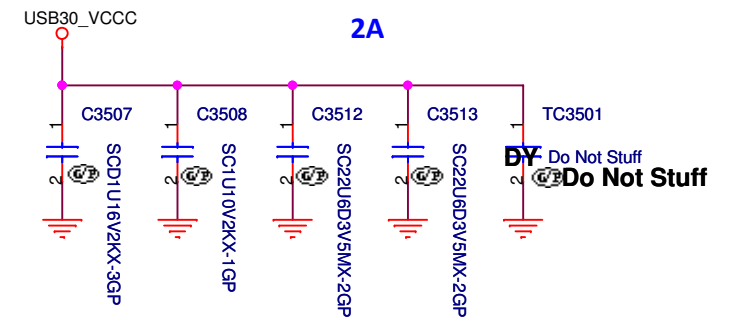
Main Func = USB3.0

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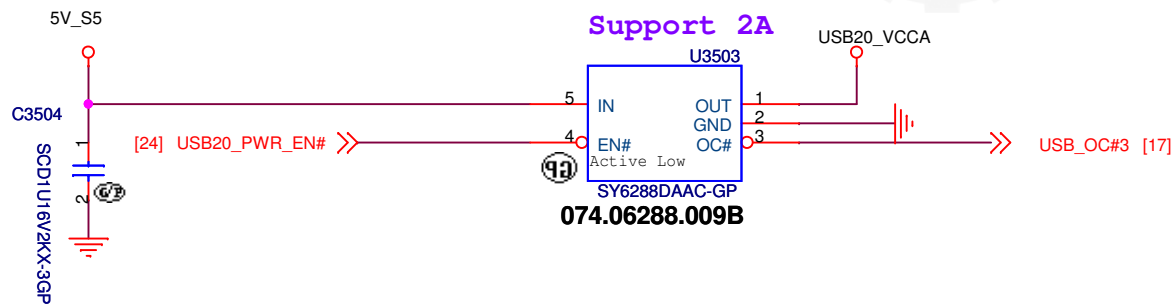


USB3.0 Port1/2

Layout Note: Close USB1

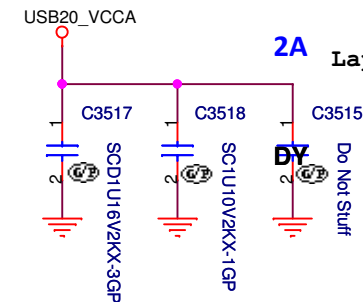


Main Func = USB2.0



USB2.0 Port3 (IO Board)

Layout Note: Close CON1



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Title

USB Power SW

Size

Document Number

Turis STR (FT4)

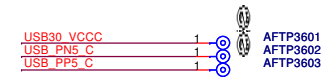
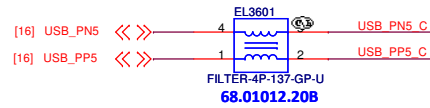
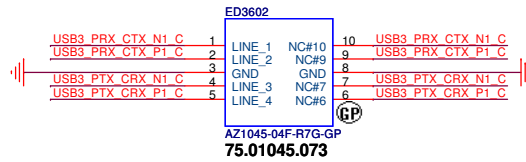
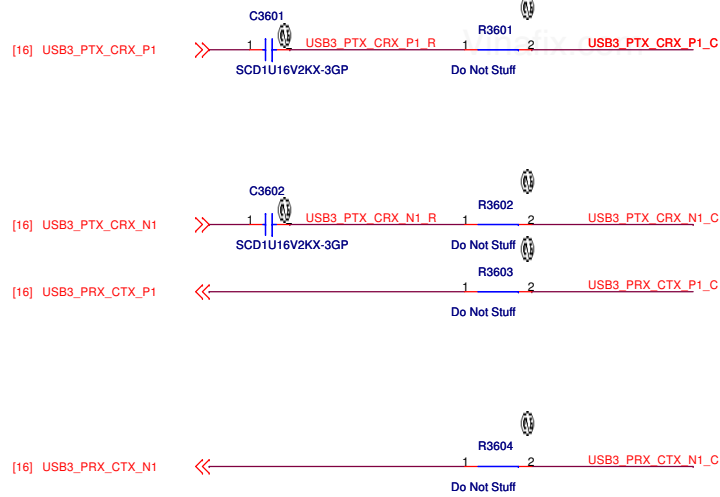
Rev

A00

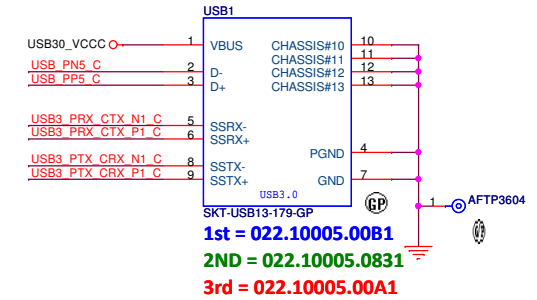
Date: Monday, August 29, 2016

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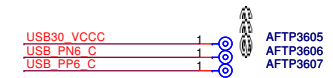
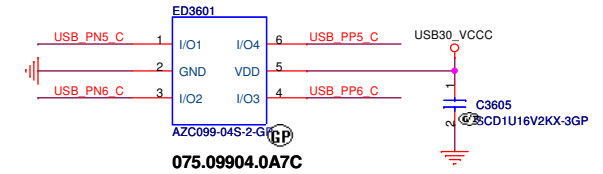
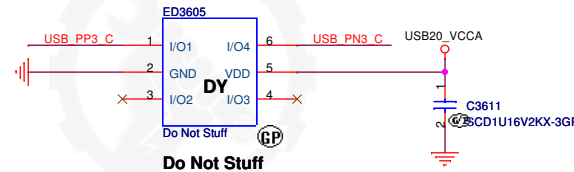
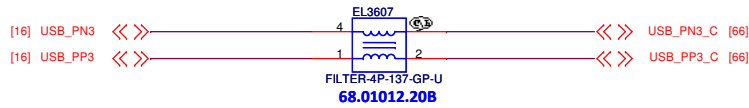
Main Func = USB3.0 Port1/2



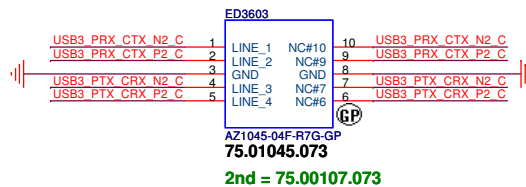
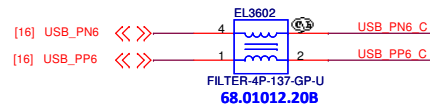
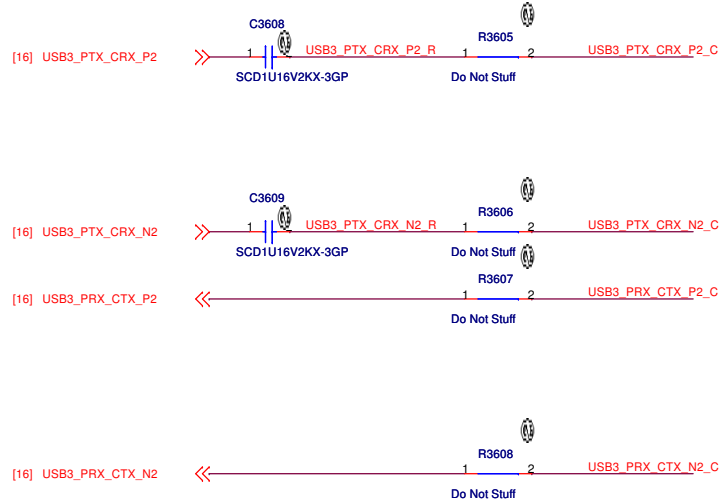
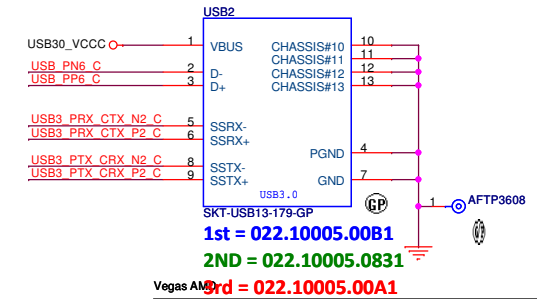
USB3.0 Port1



USB2.0 Port3



USB3.0 Port2



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Title **USB PORT1~3**

Size A3 Document Number **Turis STR (FT4)** Rev **A00**

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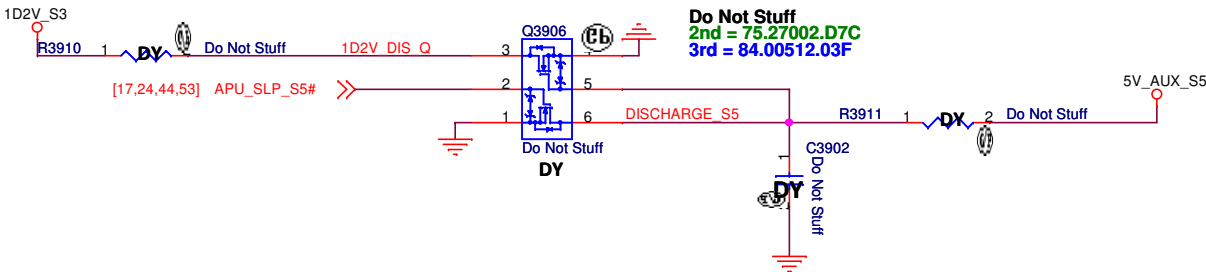
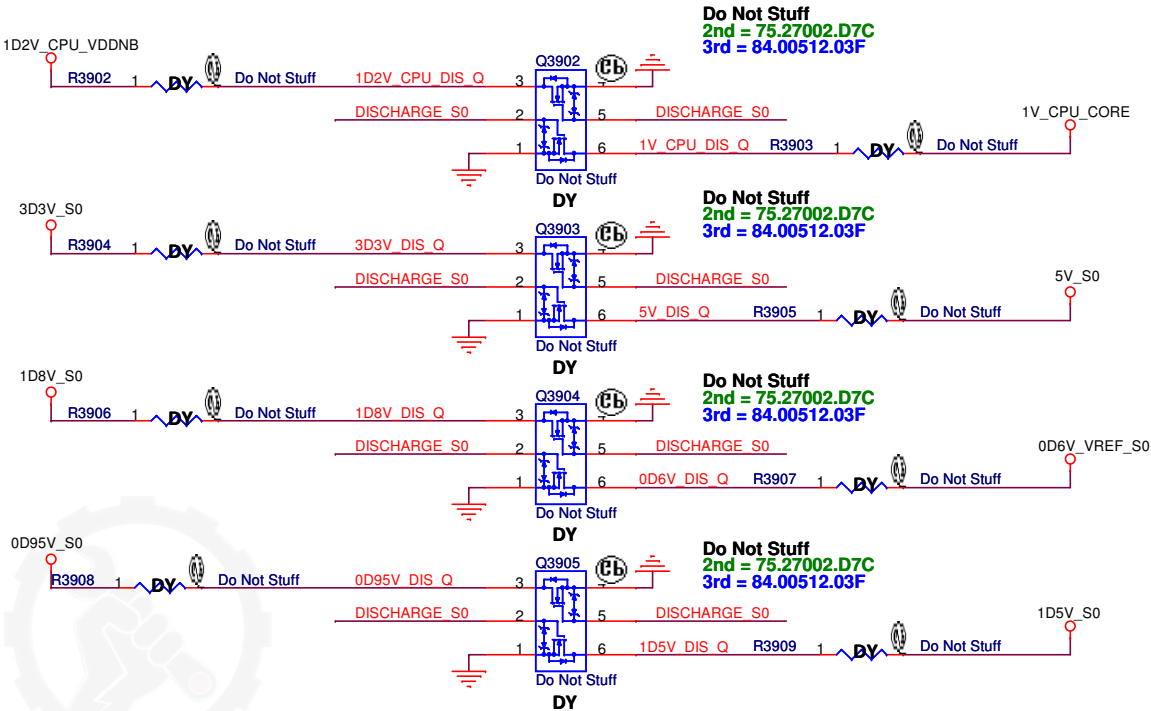
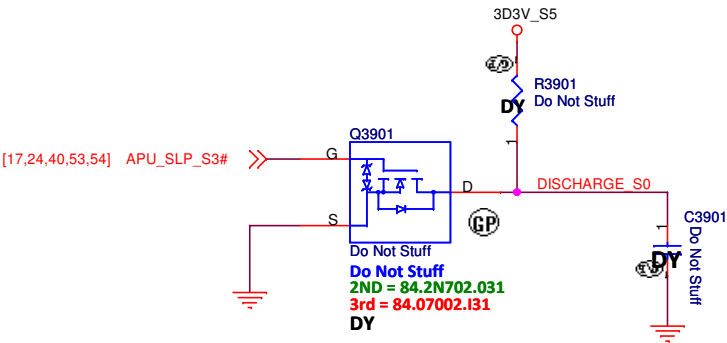
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Title (Reserved)		
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Discharge Circuit

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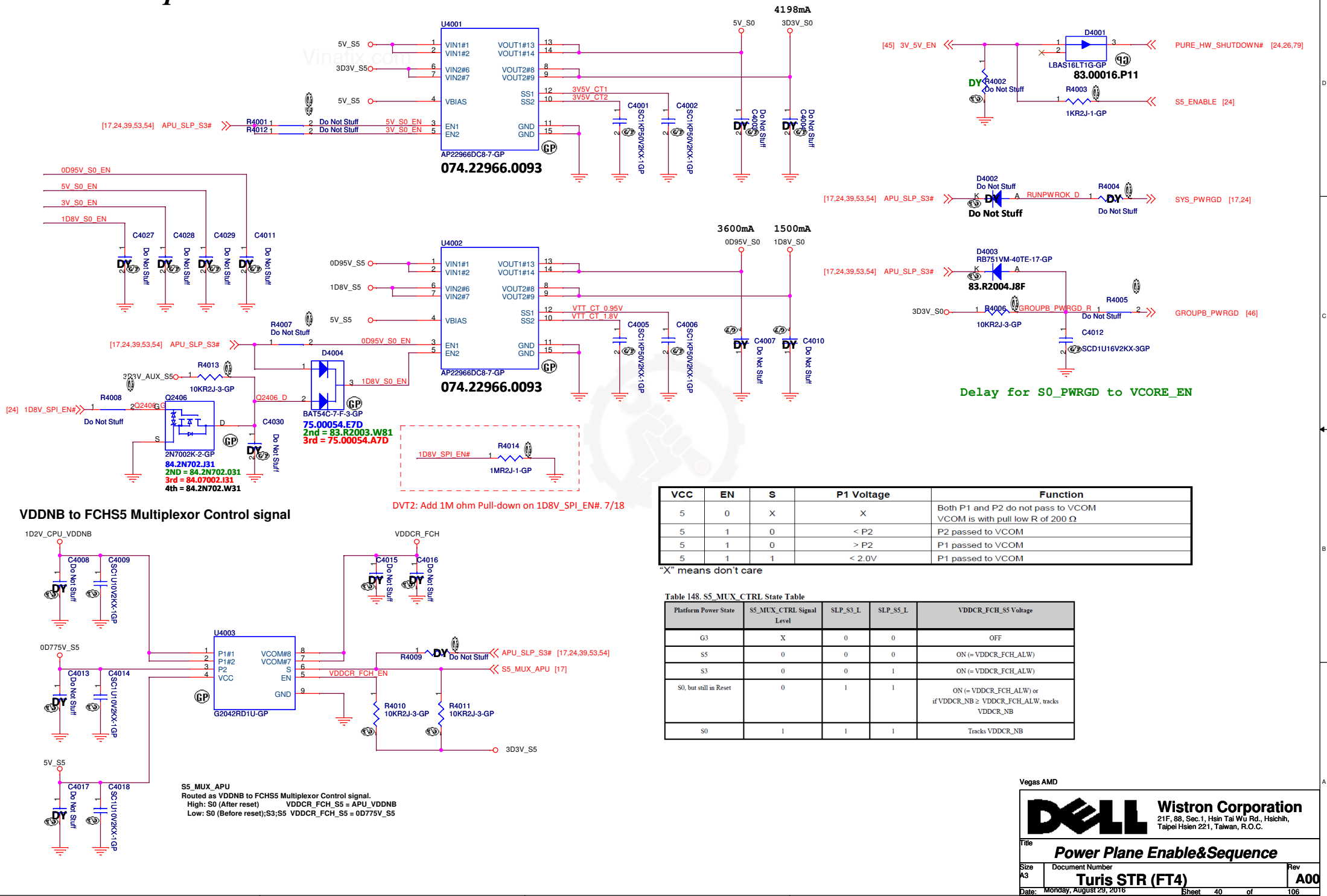
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCHARGE**

Size: Custom Document Number: **Turis STR (FT4)** Rev: **A00**

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Power Sequence



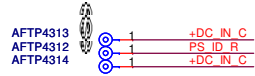
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Title (Reserved)			
Size A4	Document Number Turis STR (FT4)		Rev A00
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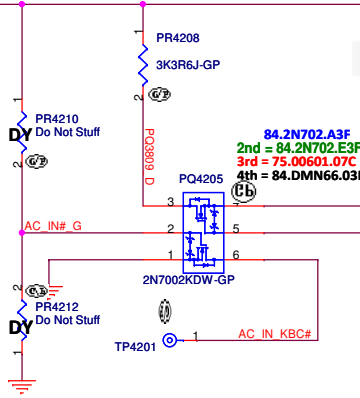
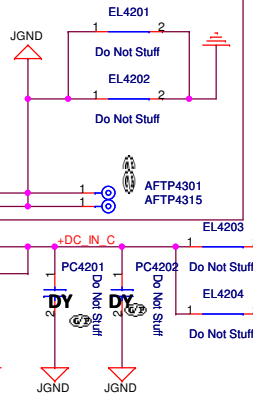
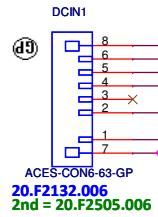
SSID = DCIN

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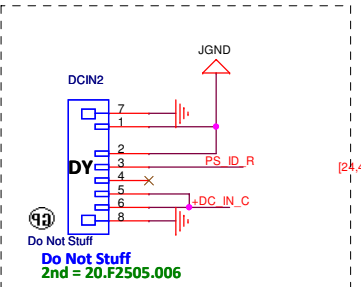
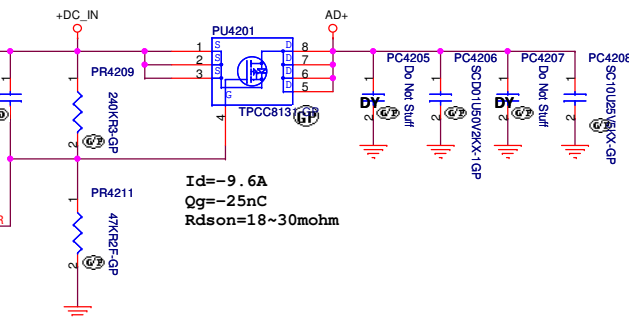
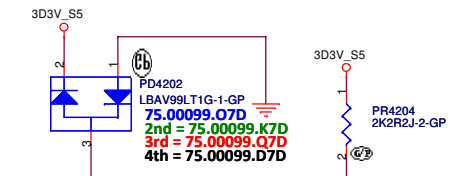
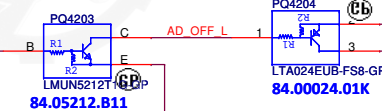
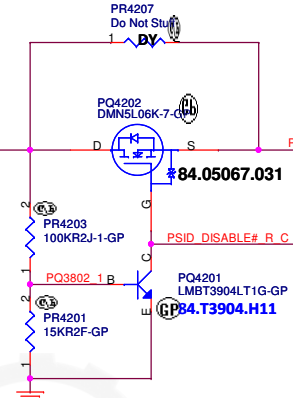


Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA



84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

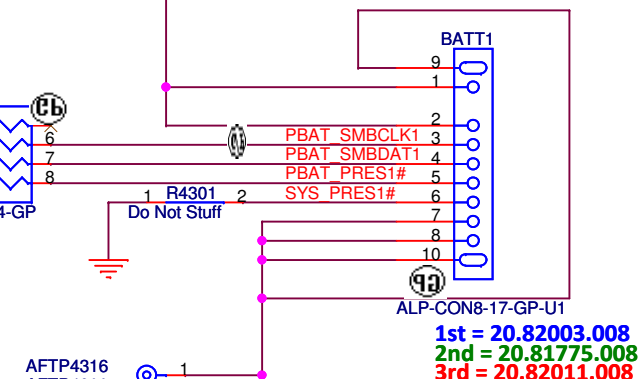
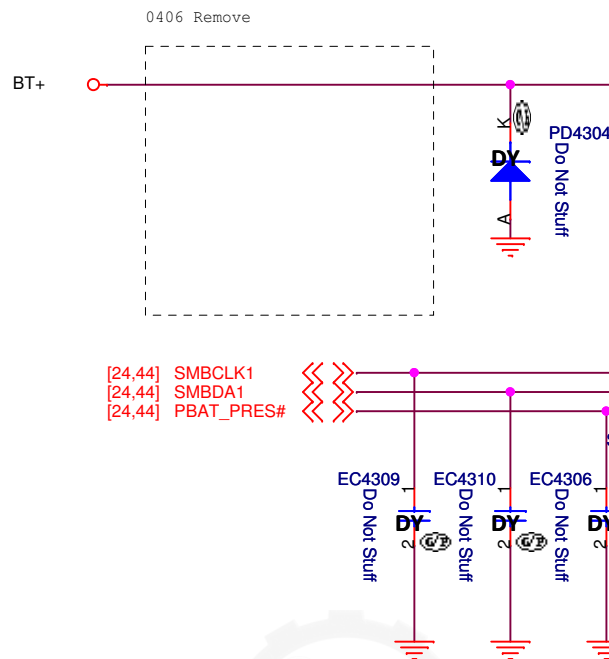
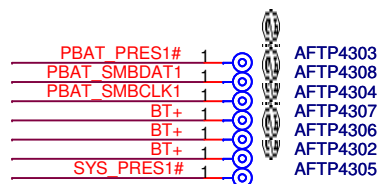


for NOVA add 1/22

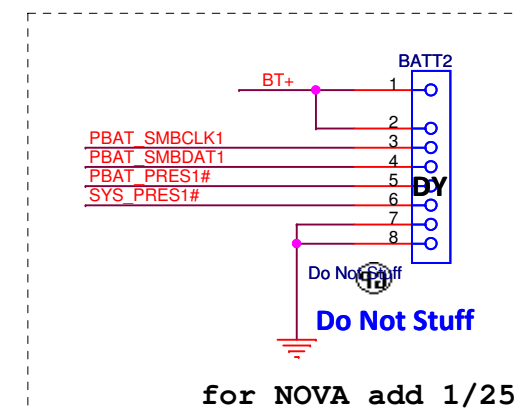
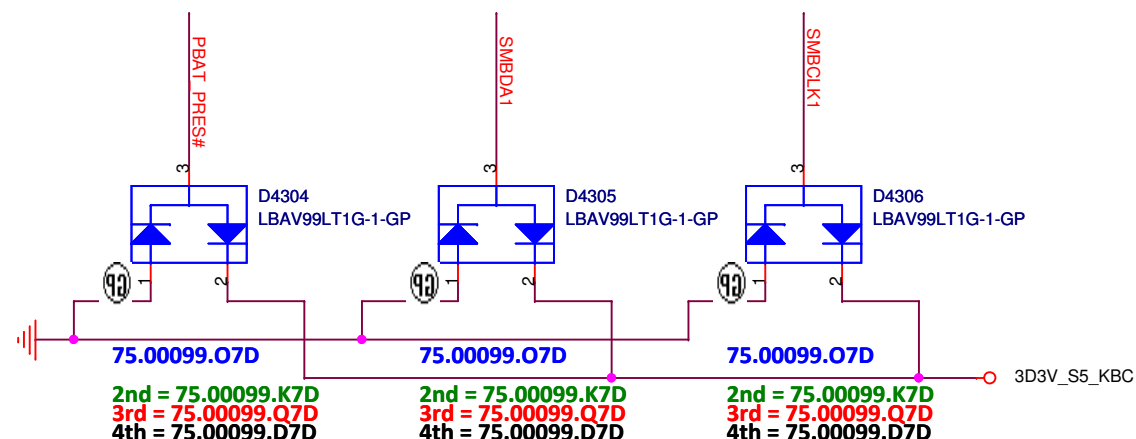
SSID = BATT CONN

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Batt Connector



Placement: Close to Batt Connector



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Title

BATT CONN

Size
A4

Document Number

Turis STR (FT4)

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Date: Monday, August 29, 2016

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```
SSID = PWR.Plane.Regulator_5v3p3v
```

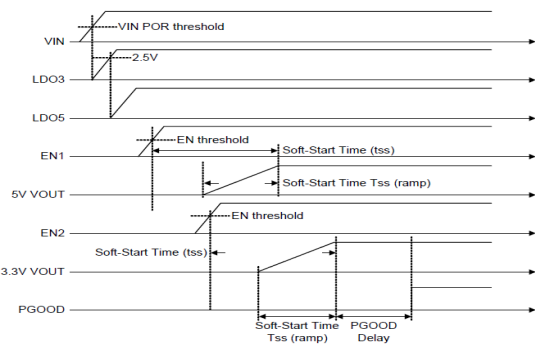
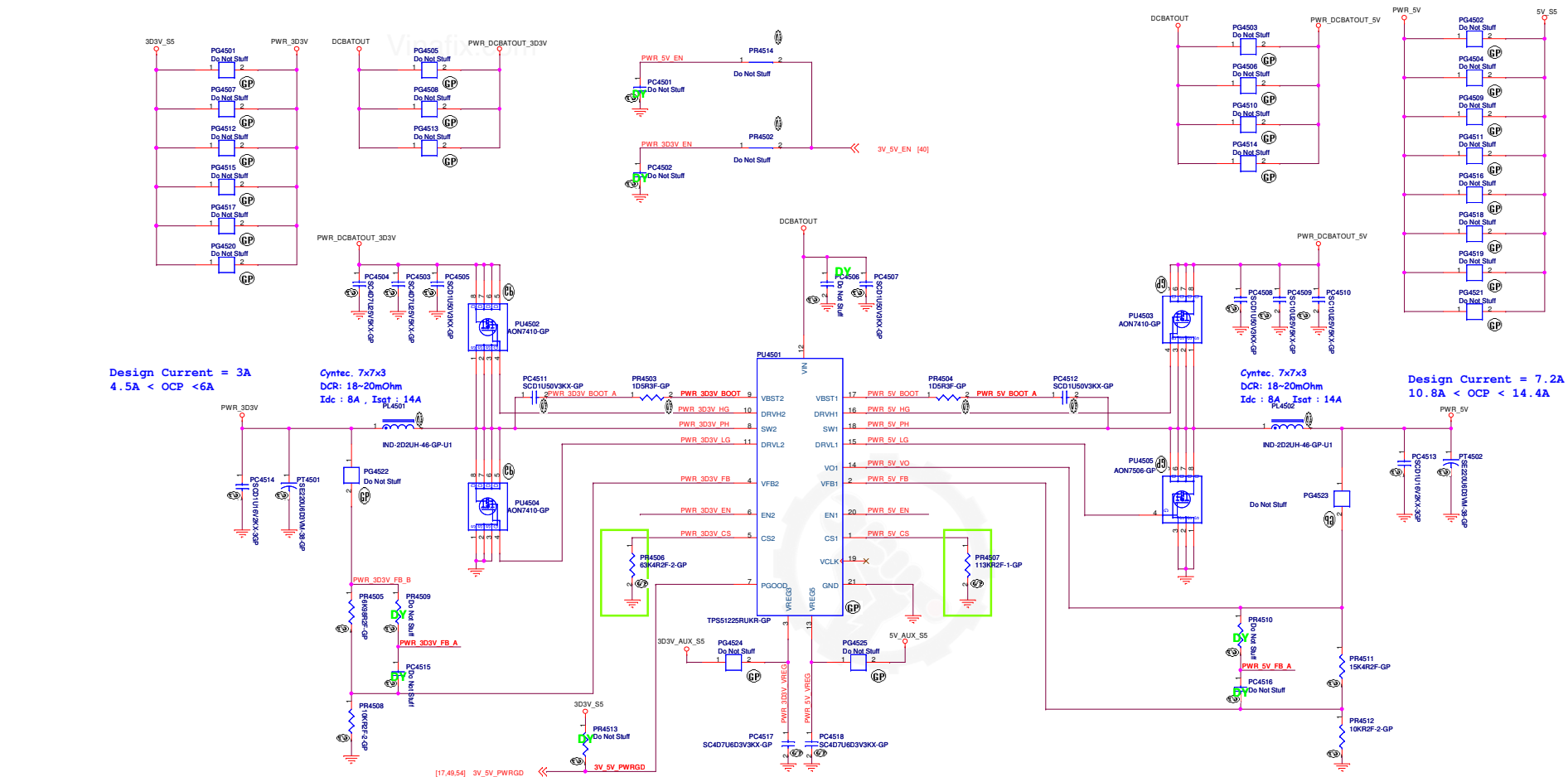
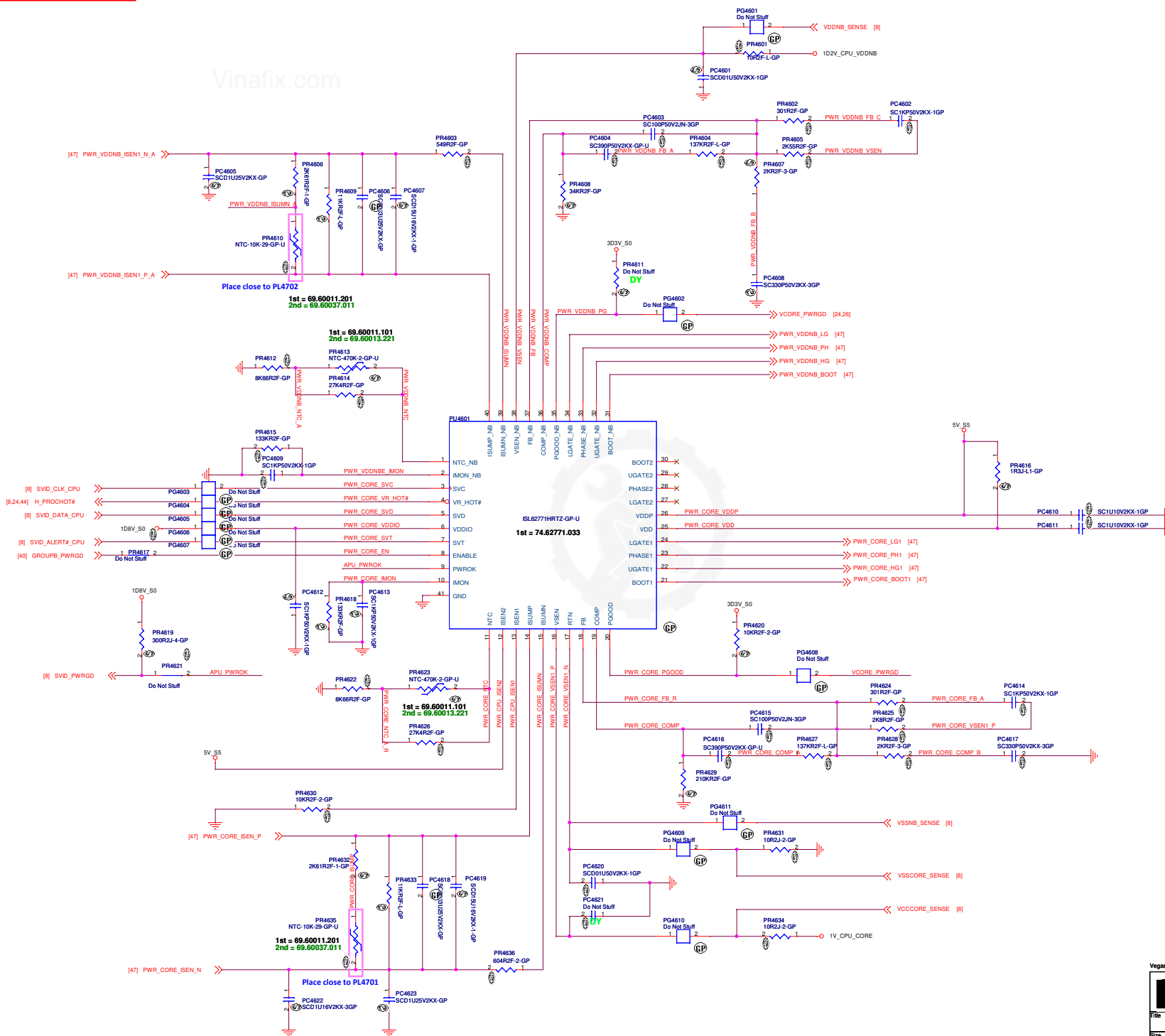
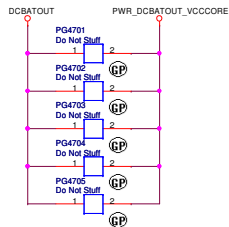


Figure 6. RT6575B Timing

```
SSID = CPU.Regulator
```



SSID = CPU.Regulator



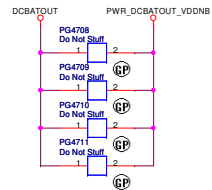
Vinafix.com

[46] PWR_CORE_HG1

[46] PWR_CORE_PH1

[46] PWR_CORE_BOOT1

[46] PWR_CORE_LG1

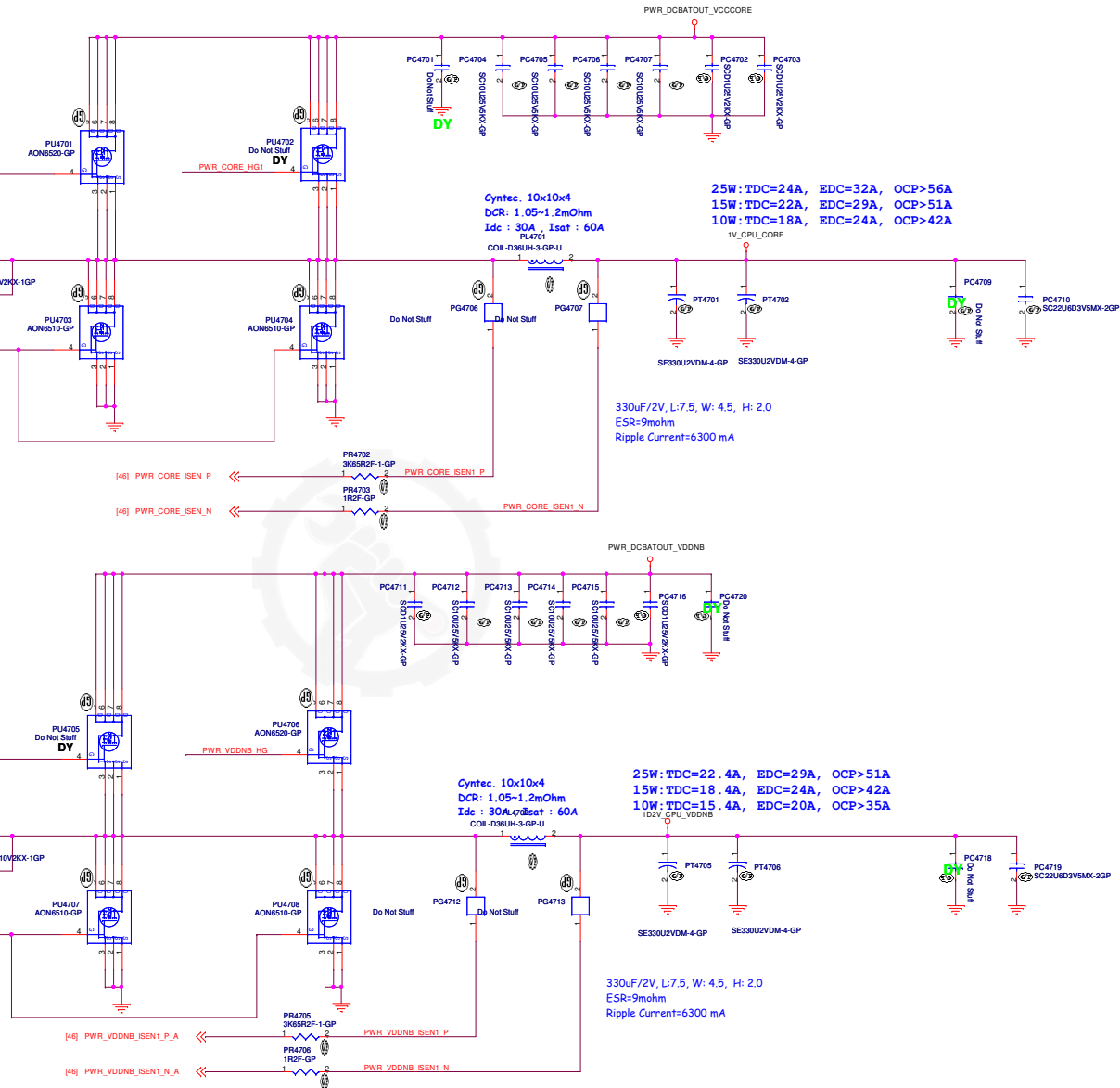


[46] PWR_VDDNB_HG

[46] PWR_VDDNB_PH

[46] PWR_VDDNB_BOOT

[46] PWR_VDDNB_LG



Vegas AMD

(Blanking)

Vegas AMD

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Title (Reserved)			
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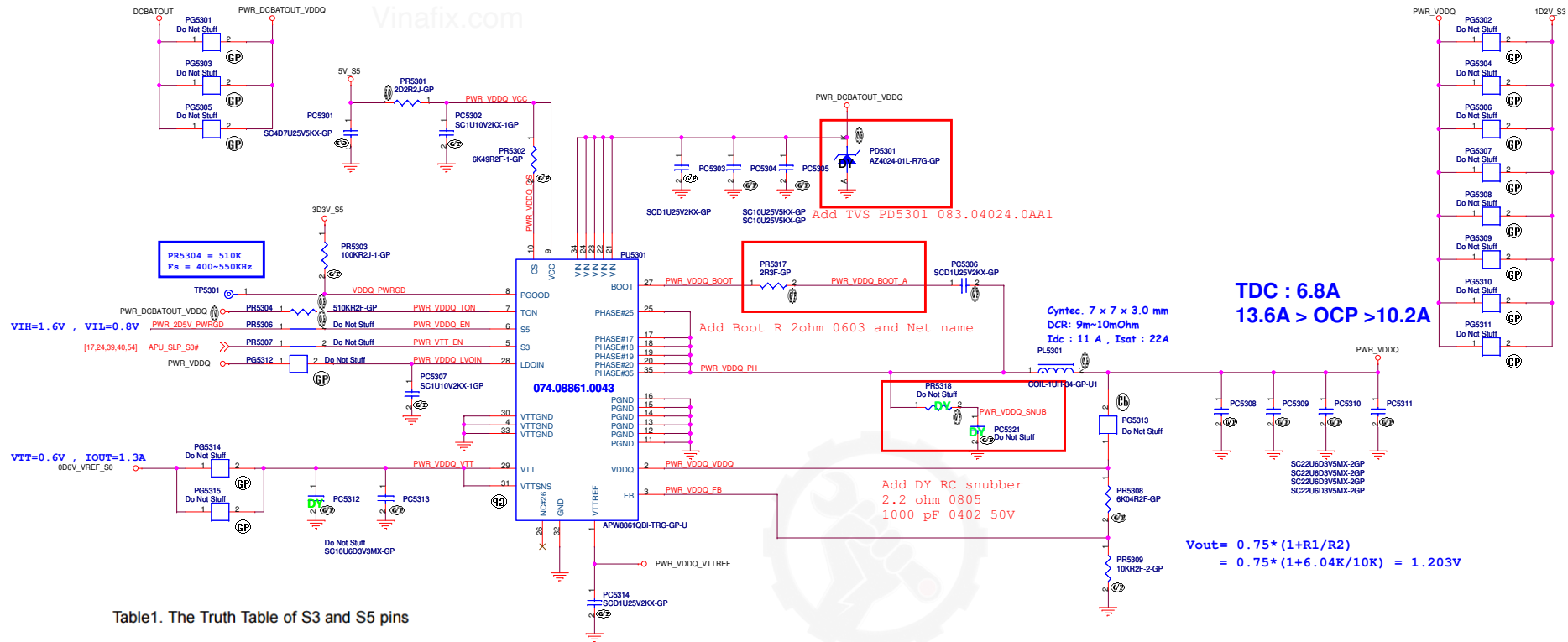
Vegas AMD

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Title (Reserved)			
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Vegas AMD

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Title (Reserved)		
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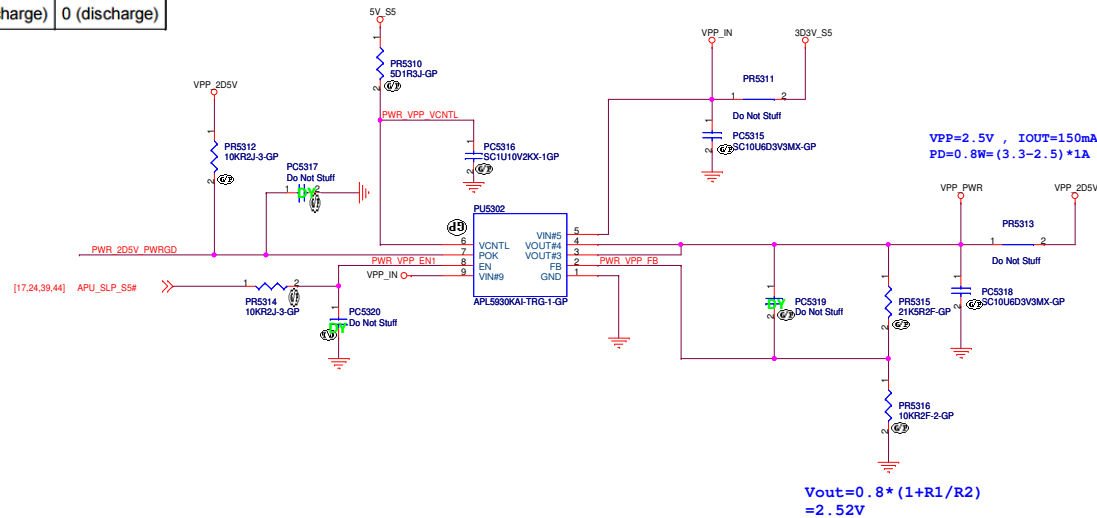


TDC : 6.8A
13.6A > OCP > 10.2A

$$V_{out} = 0.75 * (1 + R1/R2) = 0.75 * (1 + 6.04K/10K) = 1.203V$$

Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)



Vegas AMD

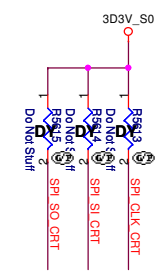
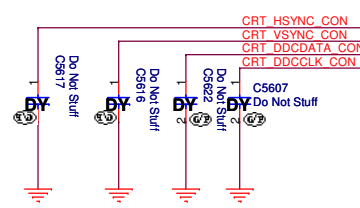
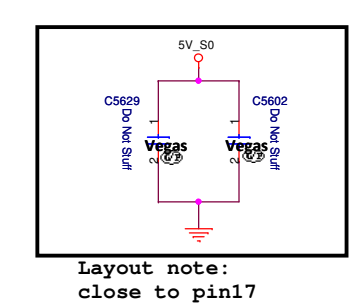
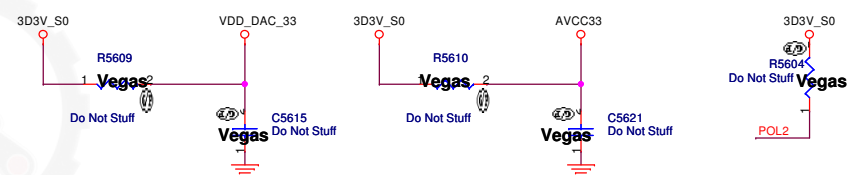
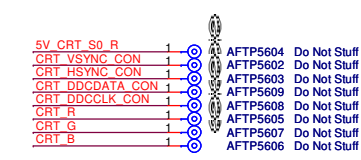
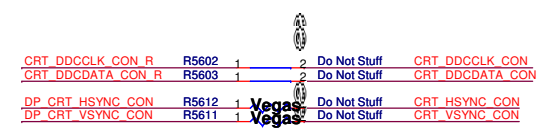
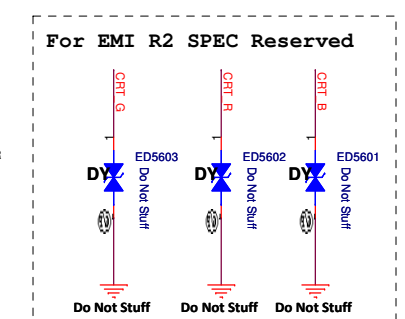
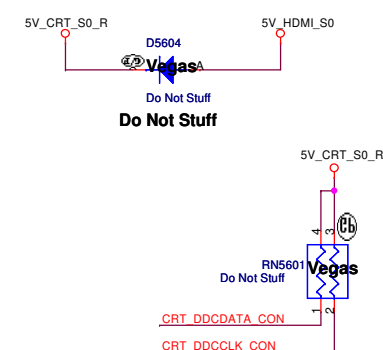
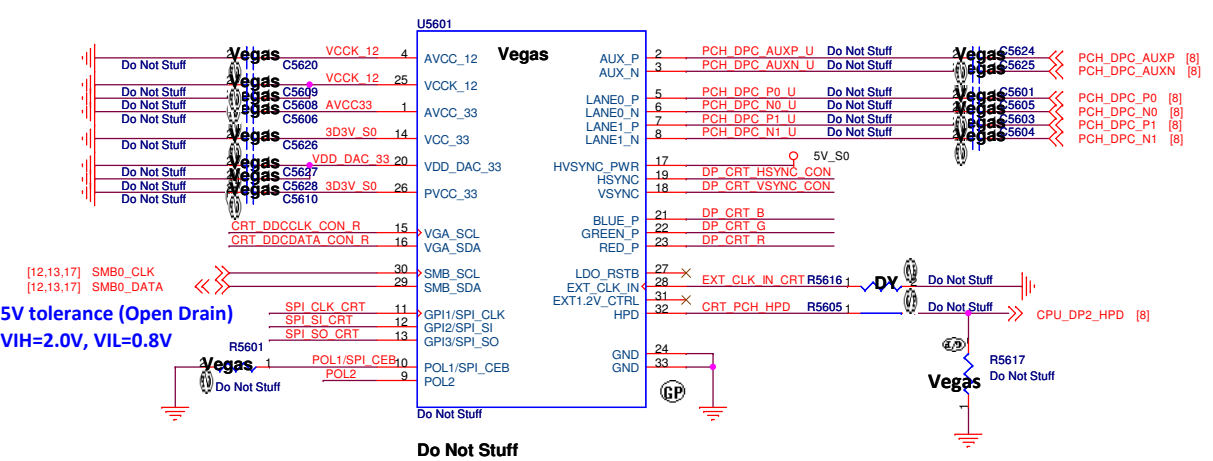
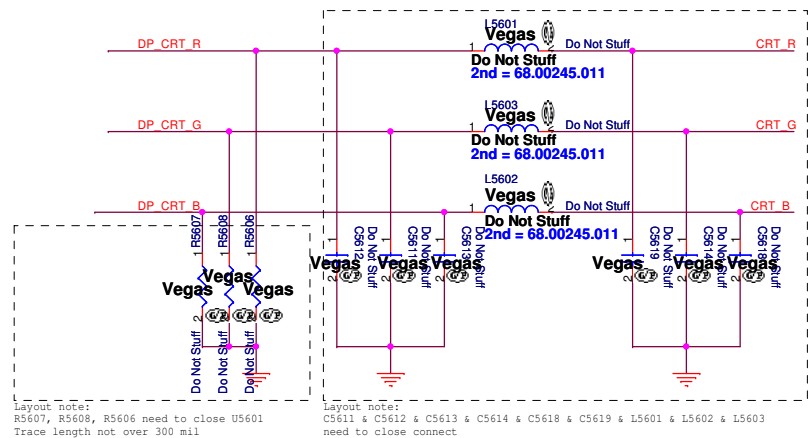
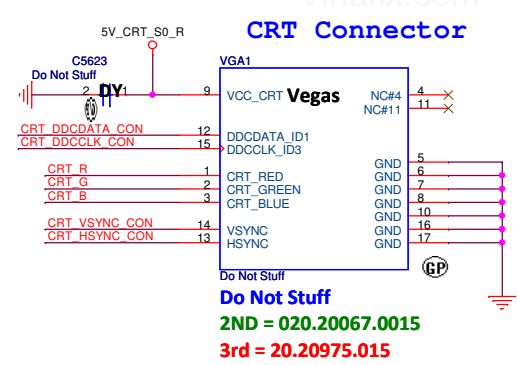
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Taipei Hsien 221, Taiwan, R.O.C.

Title **VDDQ&VTT&VPP_APW8861**

Size C Document Number **Turis STR (FT4)** Rev **A00**

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SSID = DP to VGA Converter



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	Title
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VGA

Size
A3

e	Document Number
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ment Number

Turis STR (FT4)

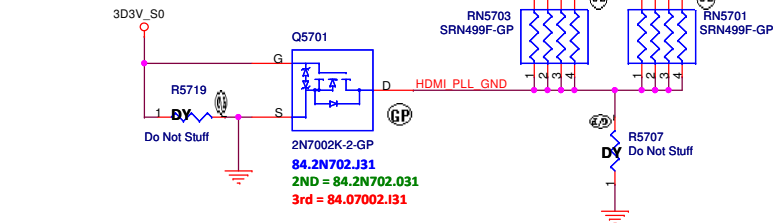
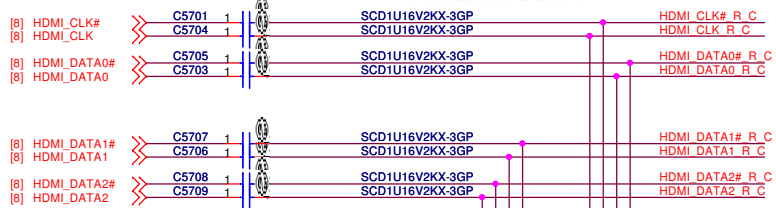
August 29, 2016 Sheet

Rev	A00
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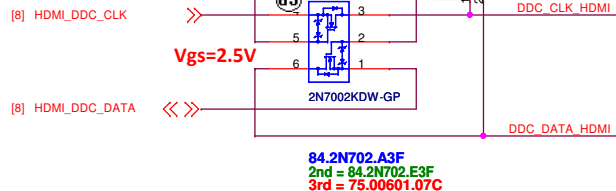
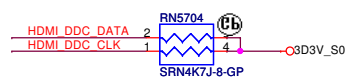
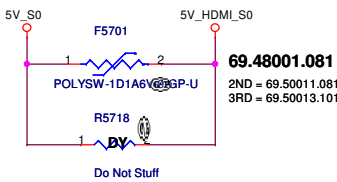
Date: Monday, August 29, 2016

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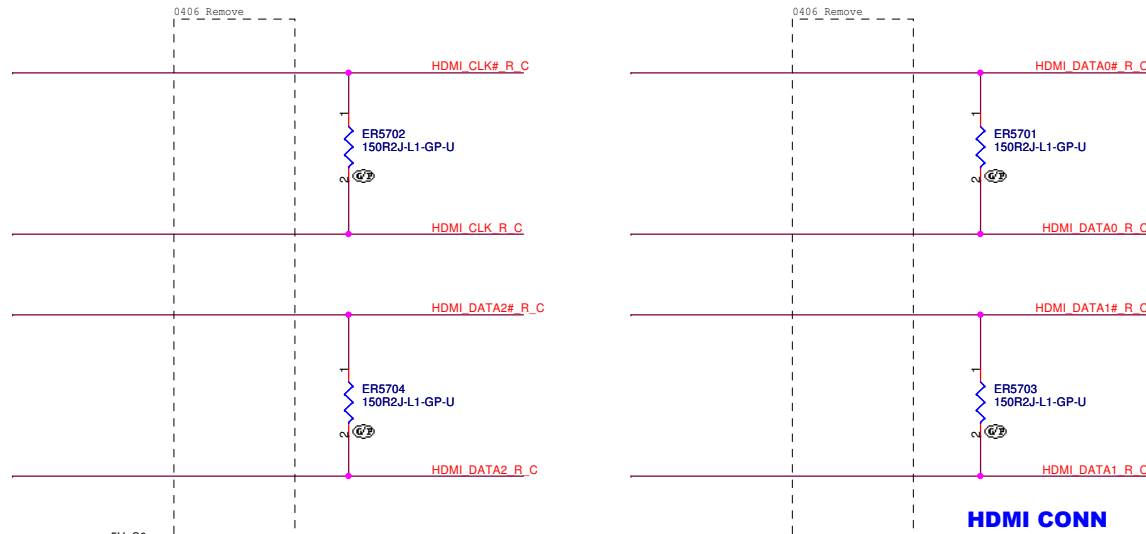
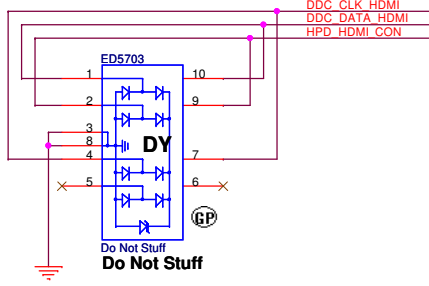
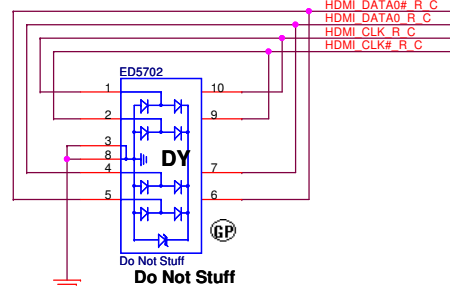
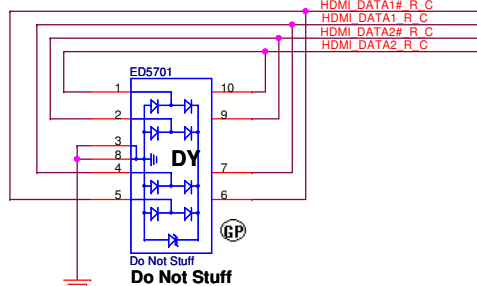
SSID = HDMI Level Shifter/Connector



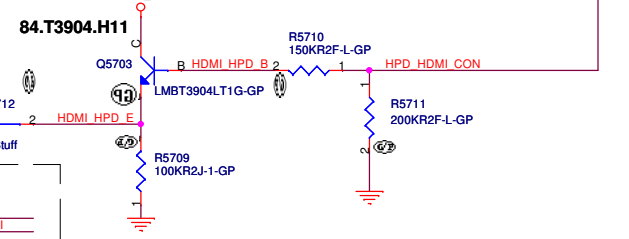
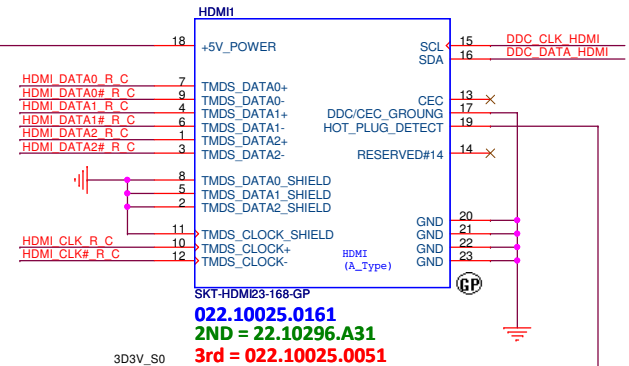
69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend



EMI Request:



HDMI CONN



(Blanking)

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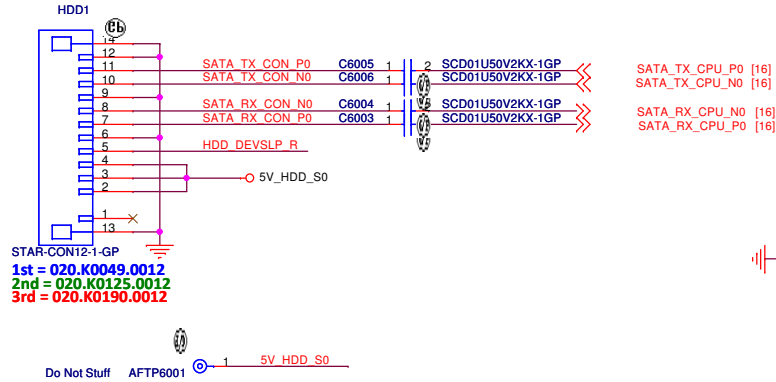
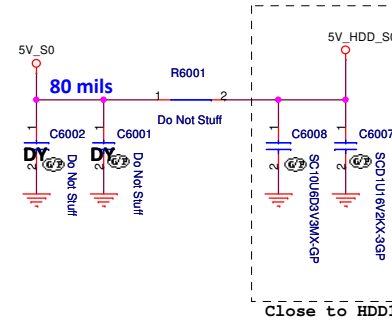
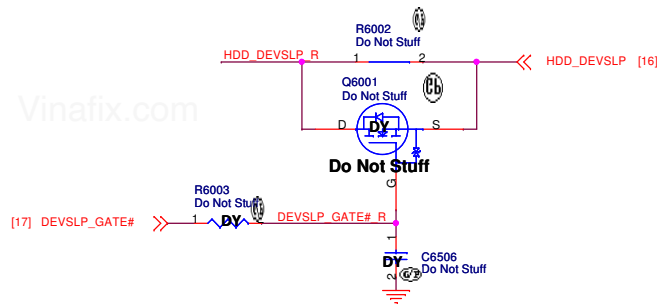
Vegas AMD

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Title (Reserved)		
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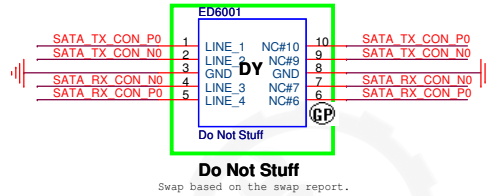
SSID = SATA

HDD Connector

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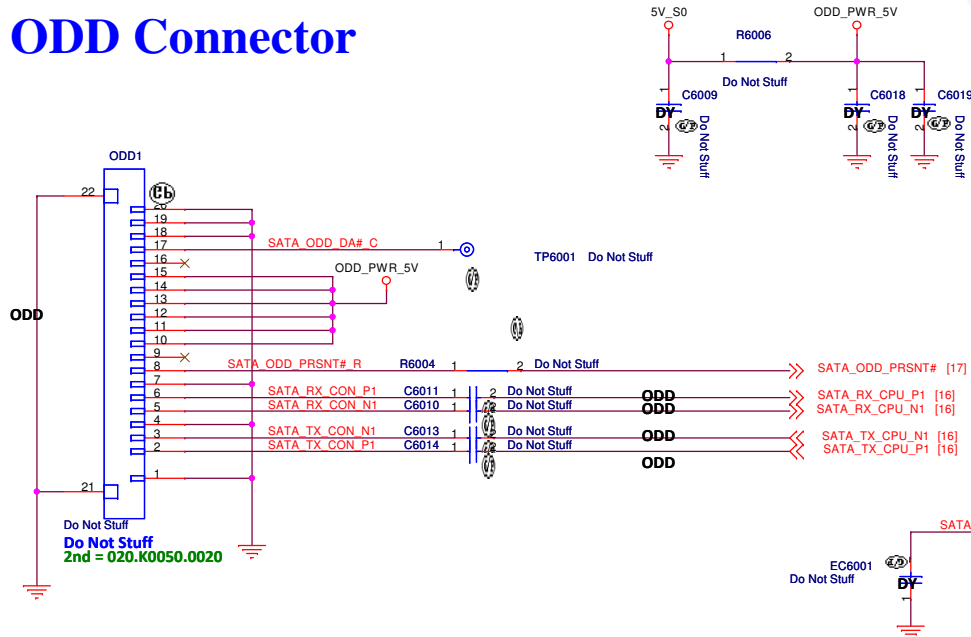


Layout Note:
Place near HDD1

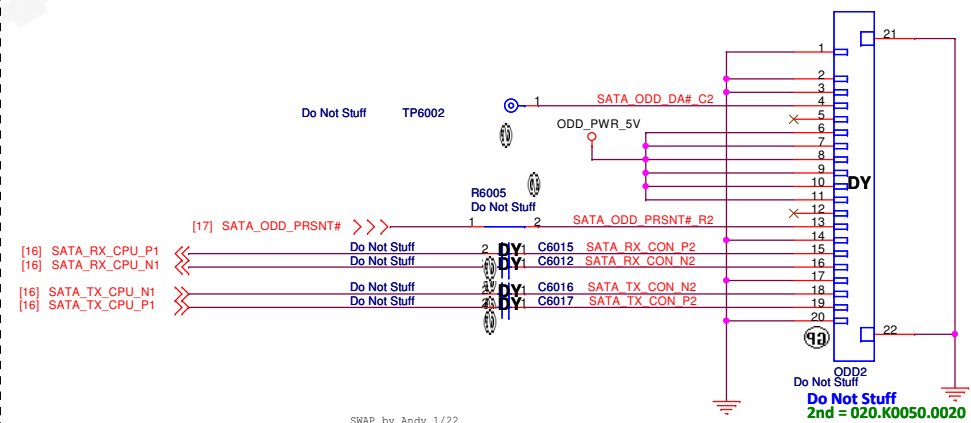


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

ODD Connector



For NOVA if use ODD2, the cable need to add on type



SWAP by Andy 1/22

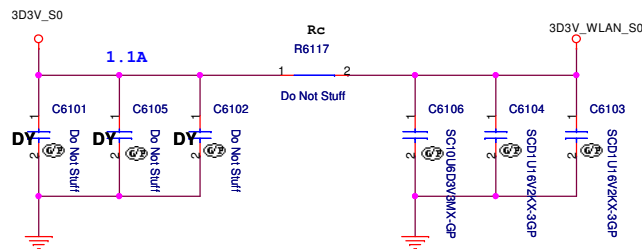
Vegas AMD

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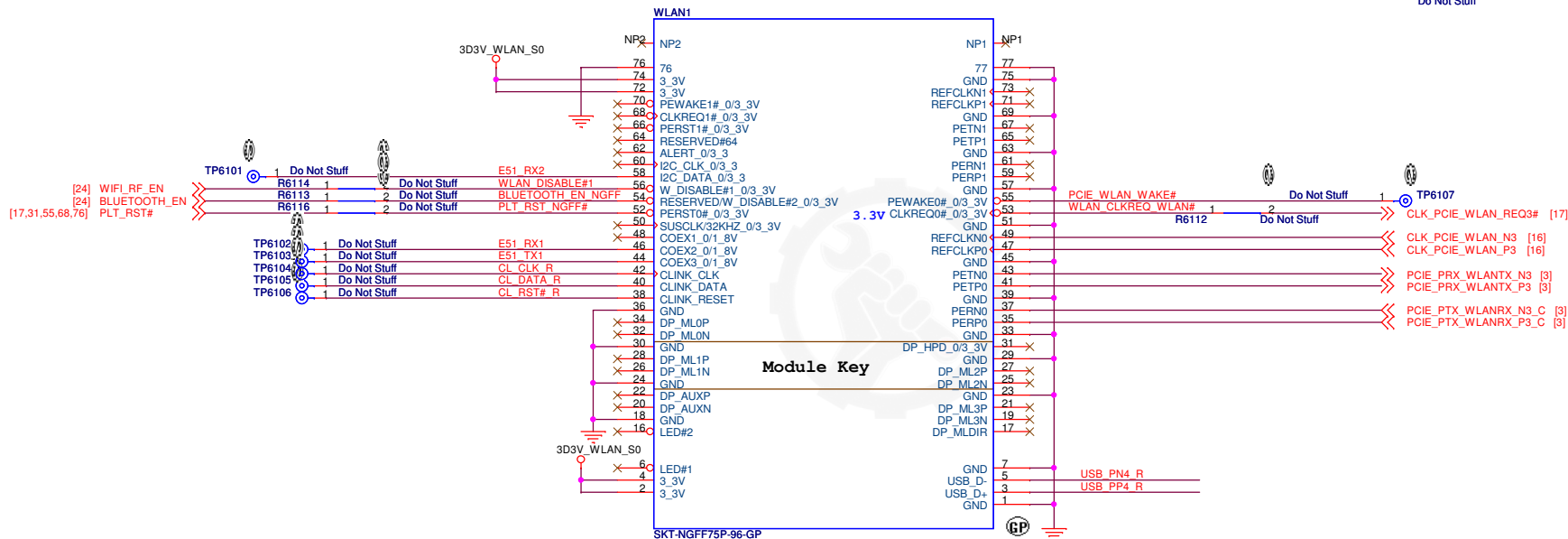
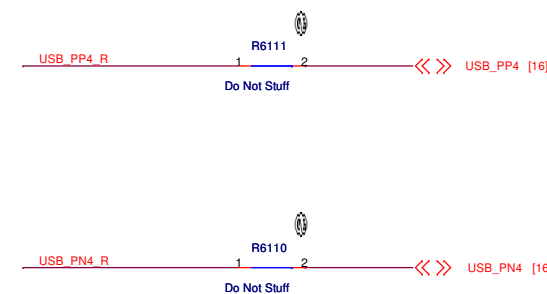
Title: **SATA IF HDD/ODD**
Size: A3 Document Number: **Turis STR (FT4)** Rev: **A00**
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Main Func = WLAN

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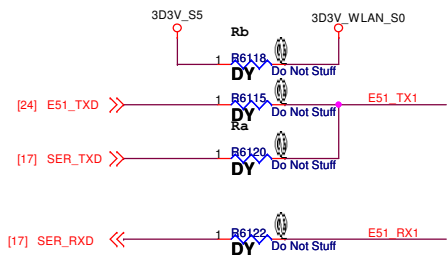


Note: pin 76 and pin 77 need contact to GND



SKT-NGFF75P-96-GP
1st = 062.10003.0621
2ND = 062.10007.0081
3rd = 062.10007.0391
4th = 62.10043.531

Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.

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File
NGFF WLAN CONN
Size A3 Document Number
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Title			
<i>Reserved</i>			
Size A4	Document Number <i>Turis STR (FT4)</i>		Rev <i>A00</i>
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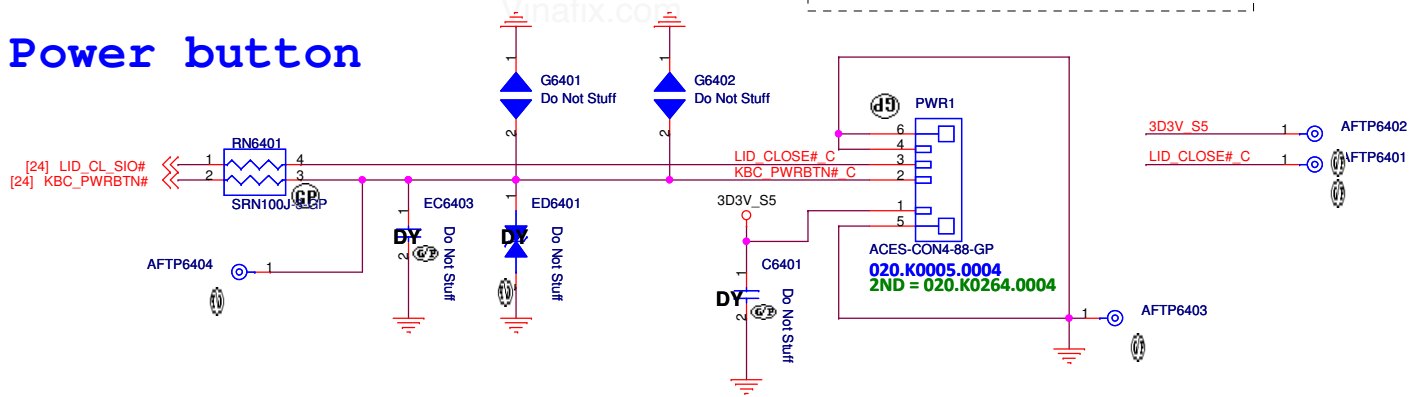
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Turis STR (FT4)		Rev A00
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SSID = LED board/Power Button

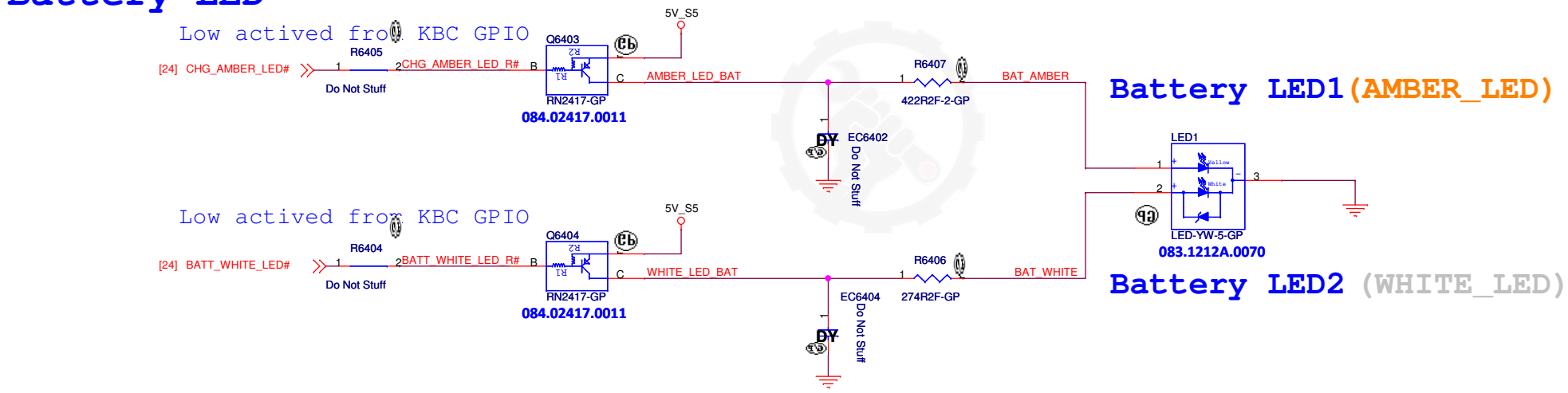
For EMI Reserved

LID_CLOSE# C EC6401 DY 2 Do Not Stuff

Power button



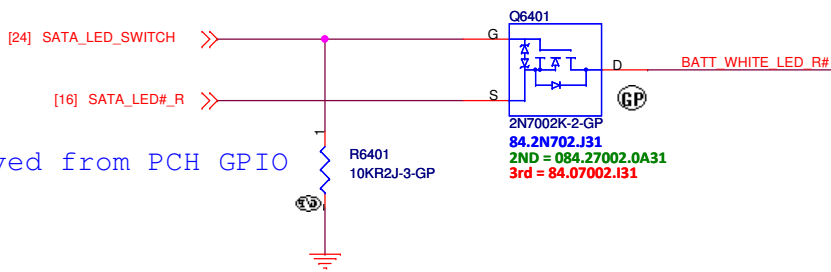
Battery LED



HDD LED

High activated from KBC GPIO

Low activated from PCH GPIO

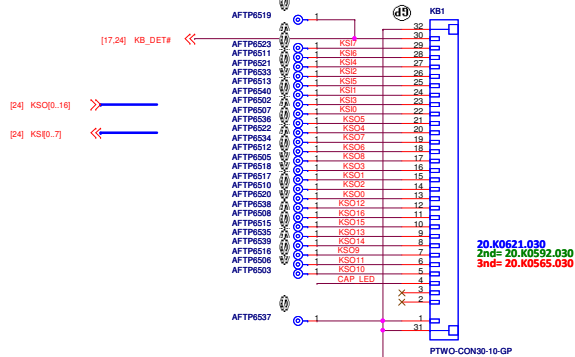


Vegas AMD

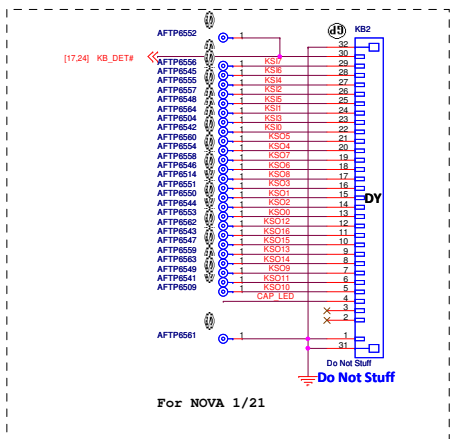
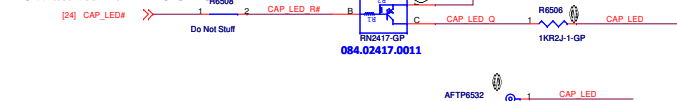
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LED Board&Power Button			
Size Custom	Document Number	Rev	
Turis STR (FT4)		A00	
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SSID = KBC

Internal Keyboard Connector



CAP LED Control



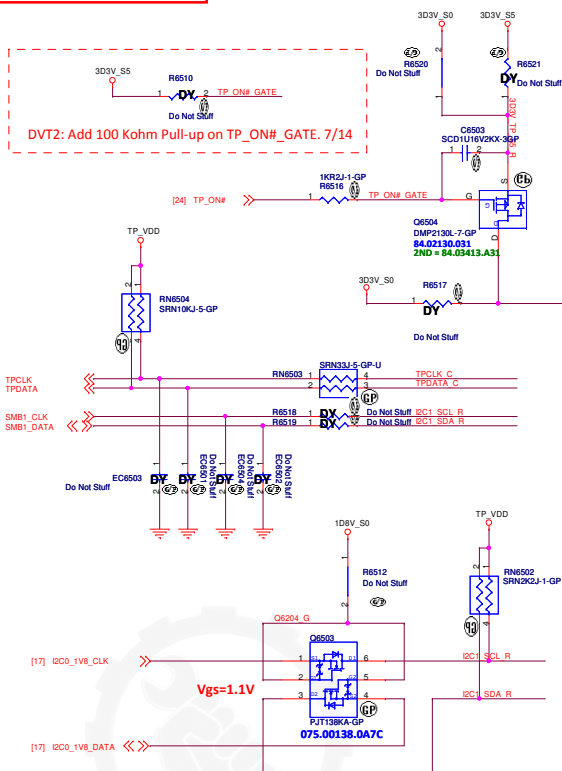
SSID = Touch.Pad

Support PTP

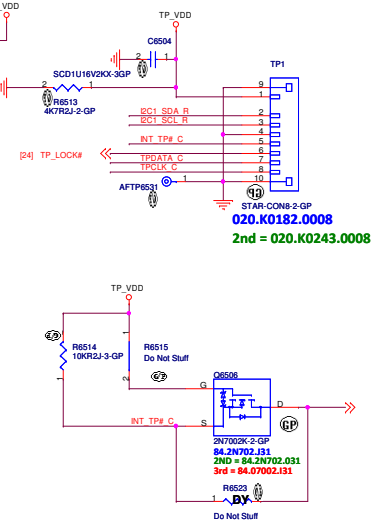
PS2

SMBUS

I2C



Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

Pin number	Pin name
1	TP_VDD
2	TPCLK_C
3	TPDATA_C
4	EC1_SCL_R
5	EC1_SDA_R
6	INT_TP#_C
7	TP_LOCK#
8	AFTP6520

Main Func = IO Connector

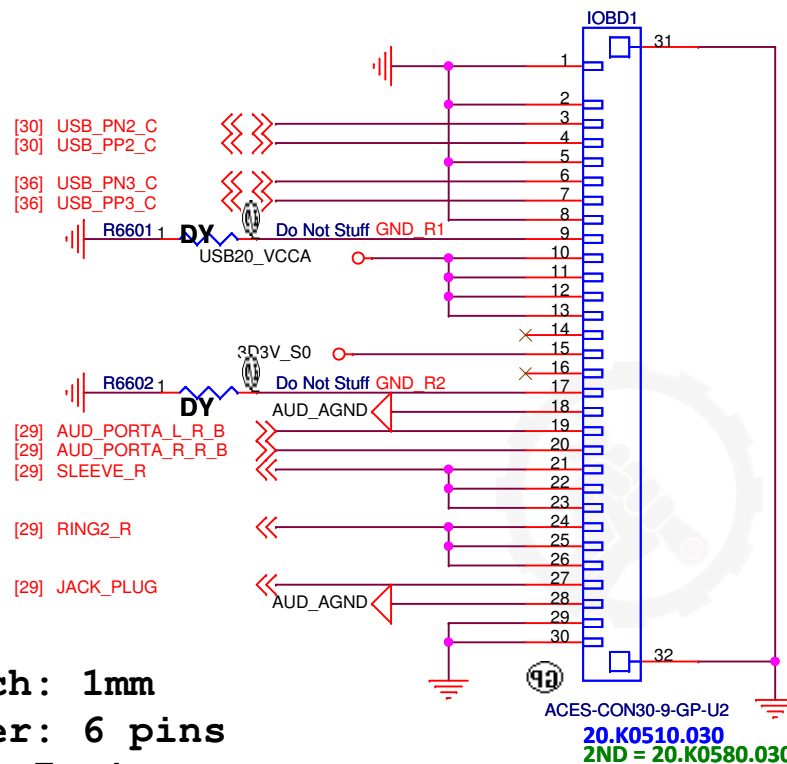
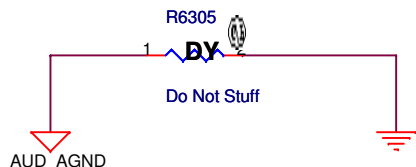
I/O Board Connector

Vinafix.com

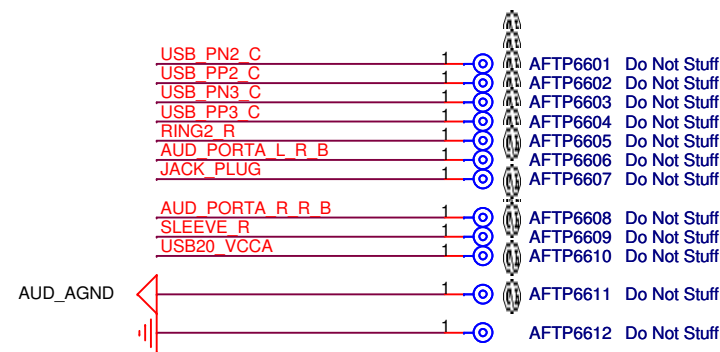
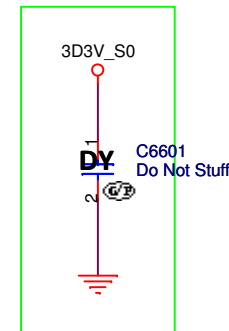
Cardreader
USB3(USB2.0)

Universal Jack

Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



2/2 Add



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Title

IO Board Connector

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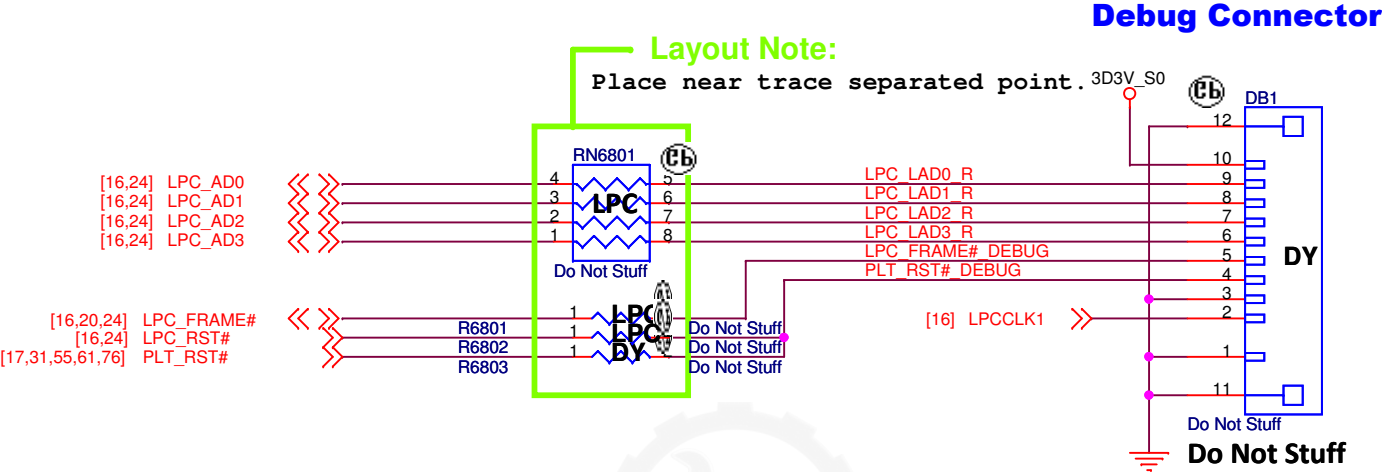
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Title (Reserved)			
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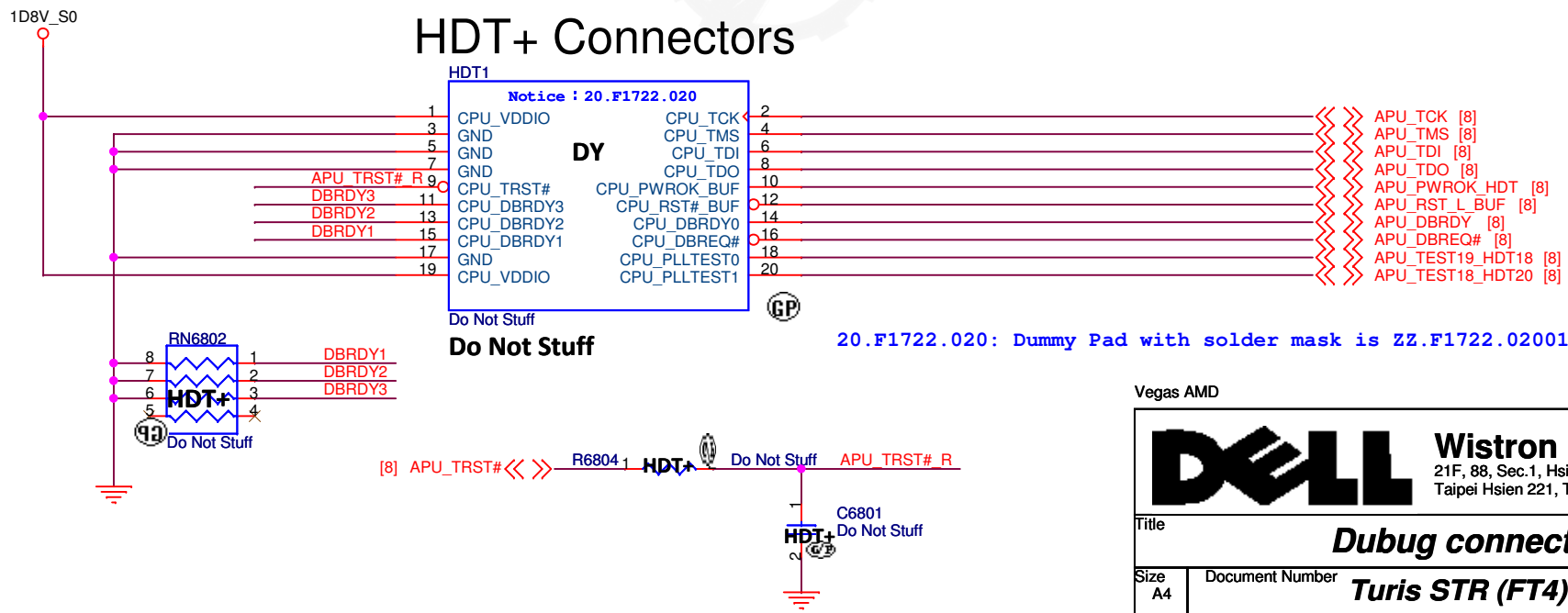
SSID = DEBUG PORT

Vinafix.com



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

HDT+ Connectors



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Title: **Dubug connector**

Size: A4 Document Number: **Turis STR (FT4)** Rev: **A00**

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Size A4	Document Number Turis STR (FT4)		Rev A00
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Title (Reserved)			
Size A4	Document Number Turis STR (FT4)		Rev A00
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GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A

1 OF 7

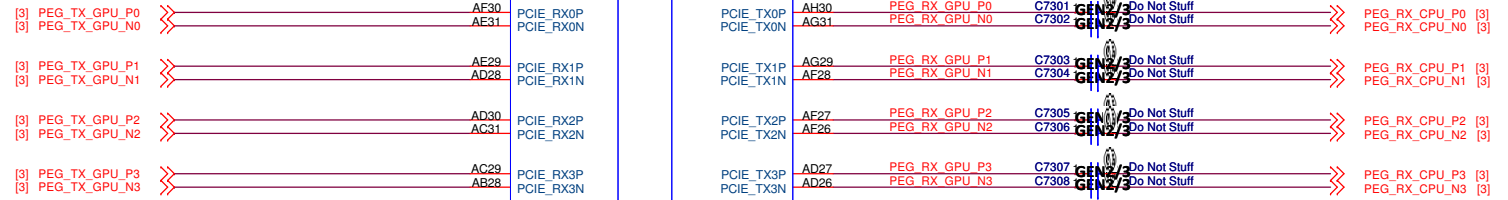
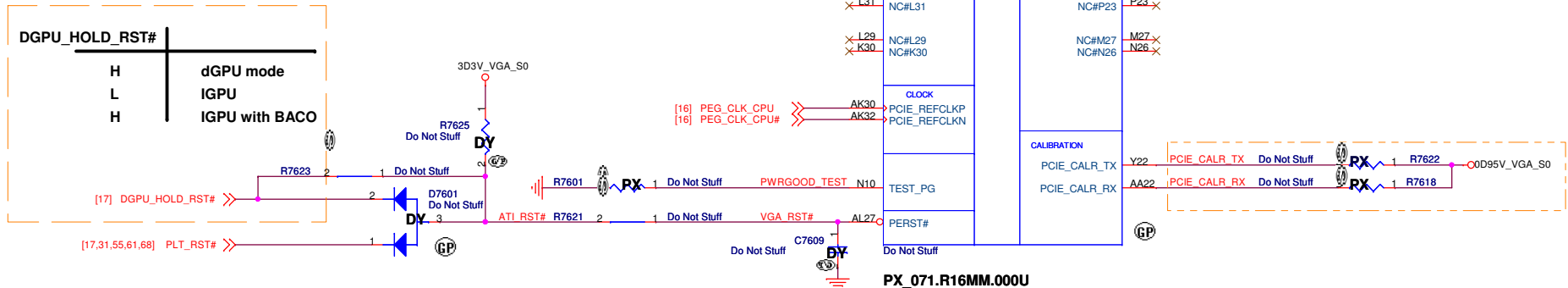


Table 3-5 PCI Express® Bus Interface

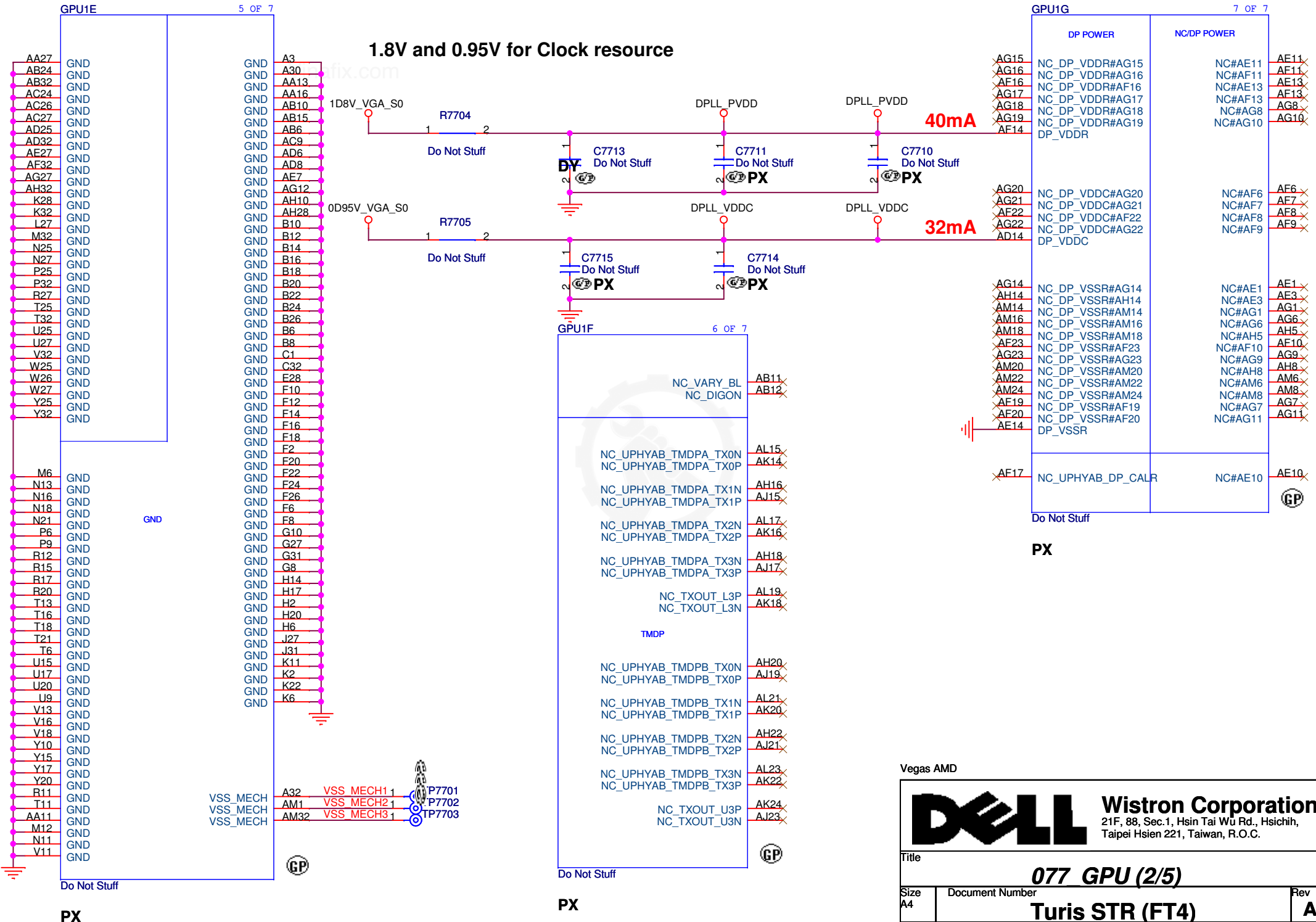
Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-k Ω (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-k Ω (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.



PX_071.R16MM.000U

Vegas AMD

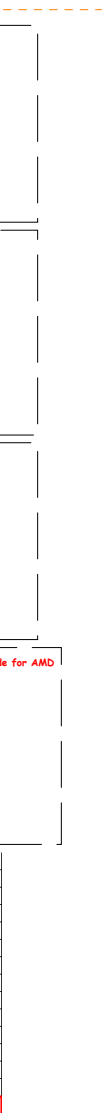
1.8V and 0.95V for Clock resource



Vegas AMD

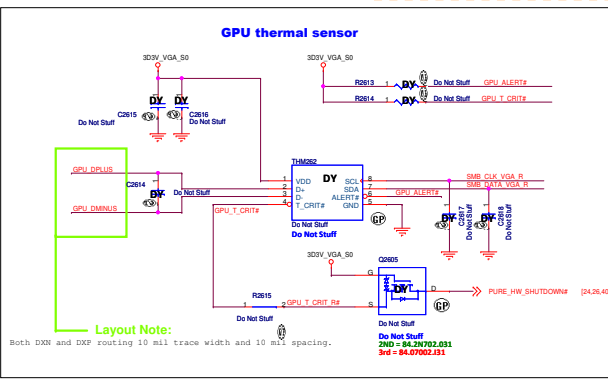


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Note :
C7501 and C7503 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.

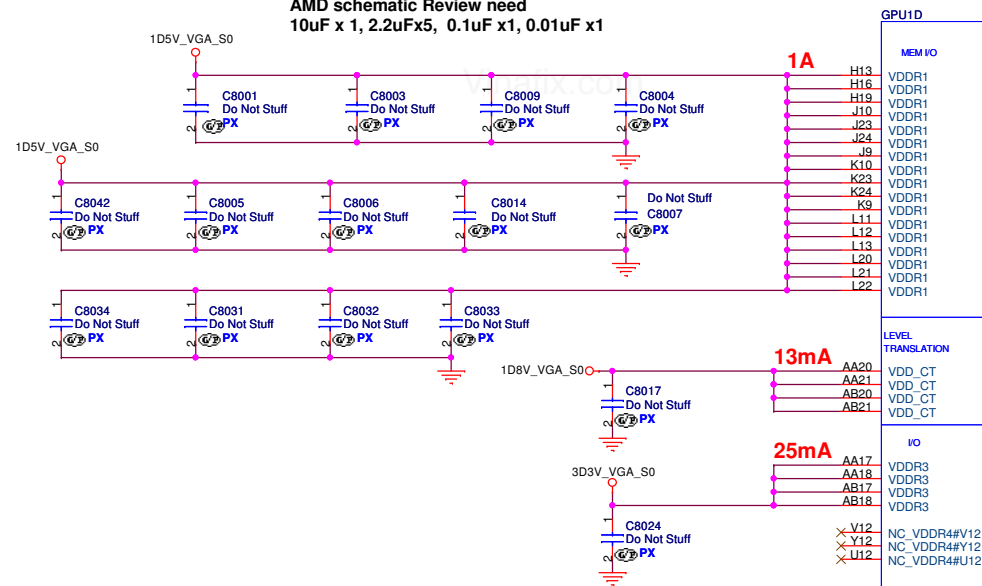
TEMPERATURE		T_CRIT#				
		2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
ALERT#	2Kohm	77	87	97	107	117
	7.5Kohm	79	89	99	109	119
	10.5Kohm	81	91	101	111	121
	14Kohm	83	93	103	113	123
	18.7Kohm	85	95	105	115	125



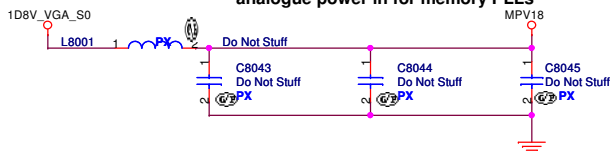
Resistor	
4.75Kohm:	PN/64.47515.6DL
4.85Kohm:	PN/64.84515.6DL
2Kohm:	PN/64.208015.6DL
4.53Kohm:	PN/64.45315.6DL
6.98Kohm:	PN/64.69815.6DL
4.99Kohm:	PN/64.49915.6DL
3.24Kohm:	PN/64.32415.6DL
3.4Kohm:	PN/64.34015.6DL
5.62Kohm:	PN/64.56215.6DL
10Kohm:	PN/64.10025.6DL

Capacitor	
680nF:	PN/78.68421.5BL
82nF:	PN/78.82321.2FL
10nF:	PN/78.10324.10L

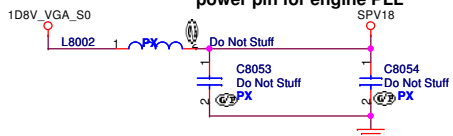
AMD schematic Review need
10uF x 1, 2.2uF x5, 0.1uF x1, 0.01uF x1



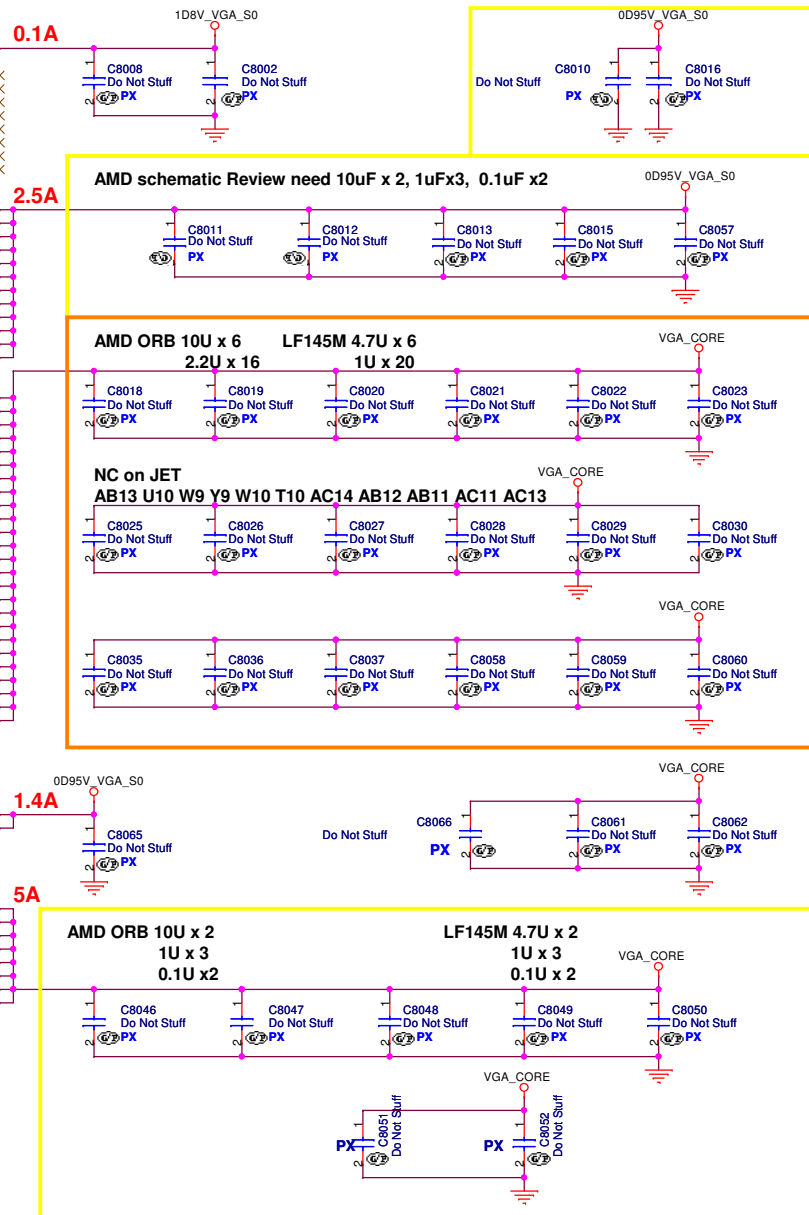
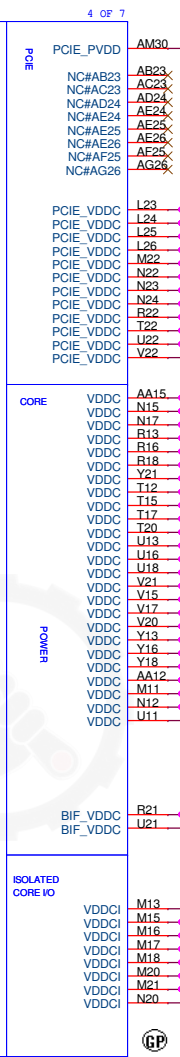
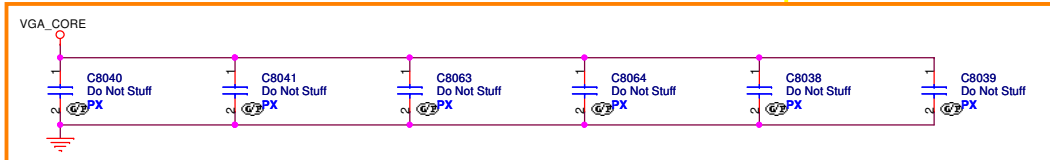
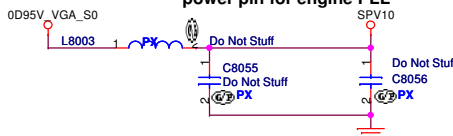
Memory phase lock loop power: Dedicated
analogue power in for memory PLLs



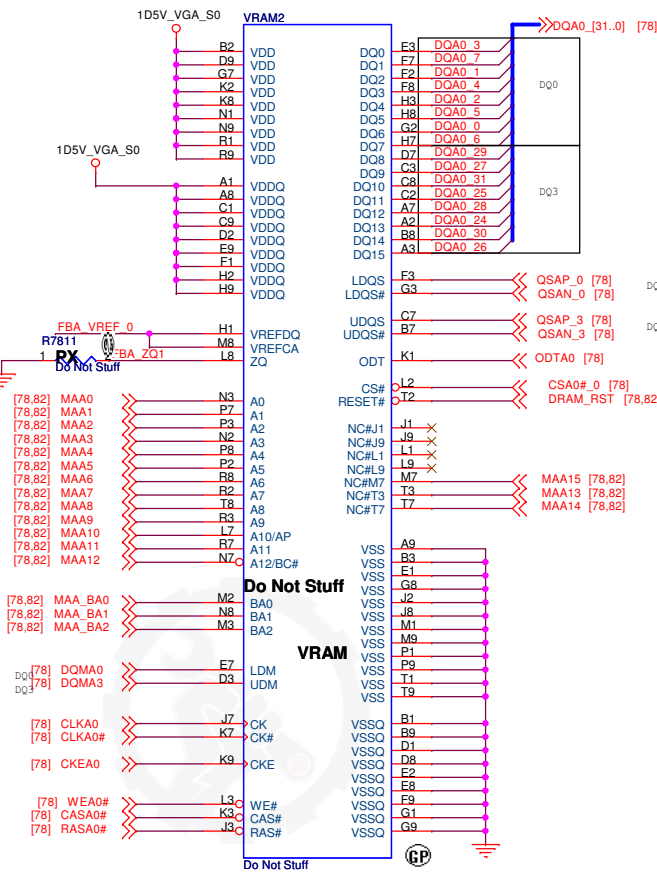
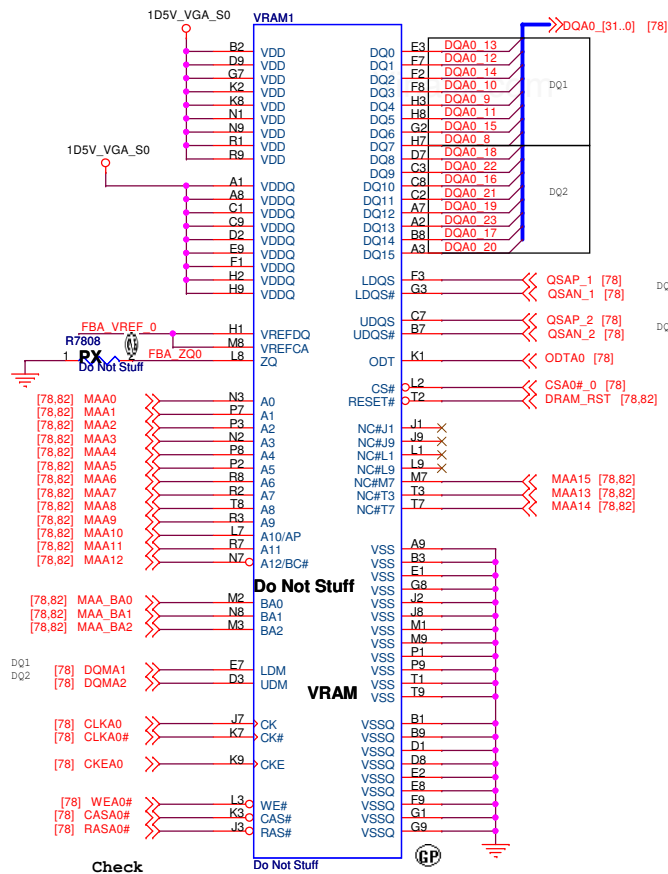
Engine phase loop power: Dedicated analogue
power pin for engine PLL



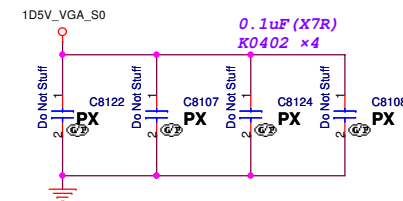
Engine phase loop power: Dedicated digital
power pin for engine PLL



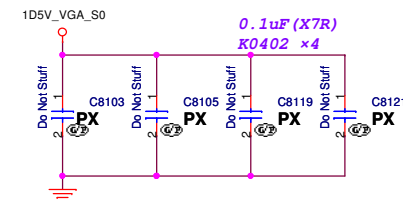
Main Func = Vram (DDR3L)



Place close VRAM1VDDQ ball

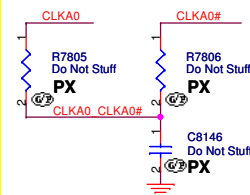


Place close VRAM2 VDD ball

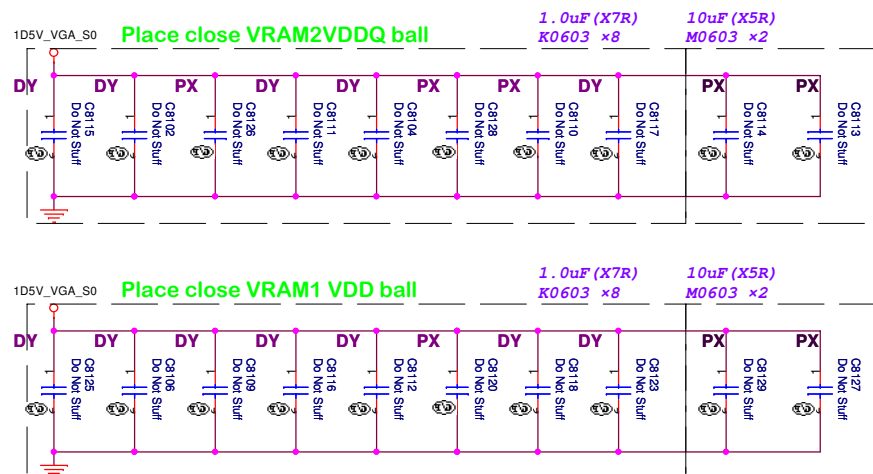
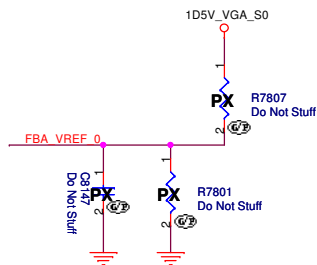


R7805 R7810

Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL

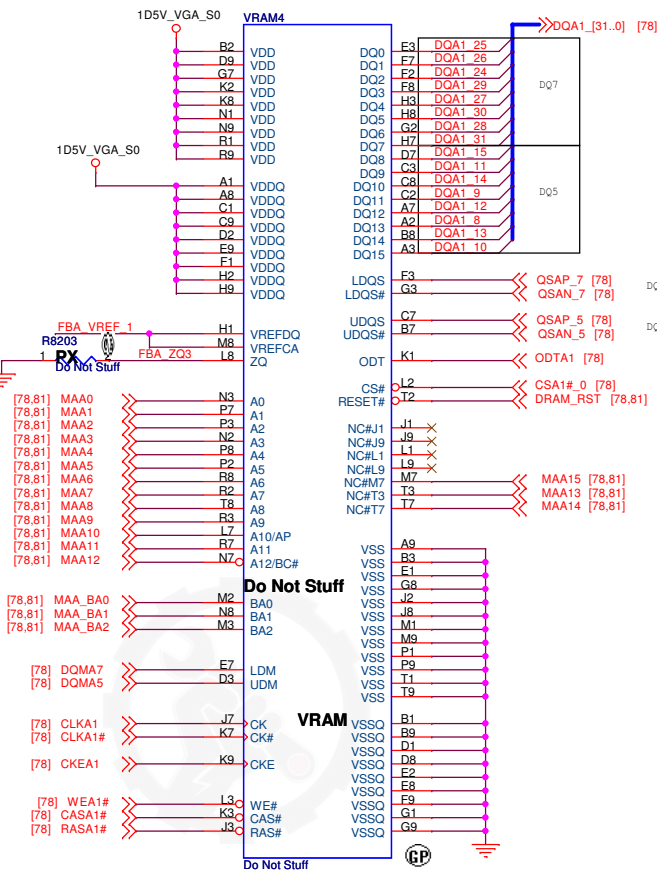
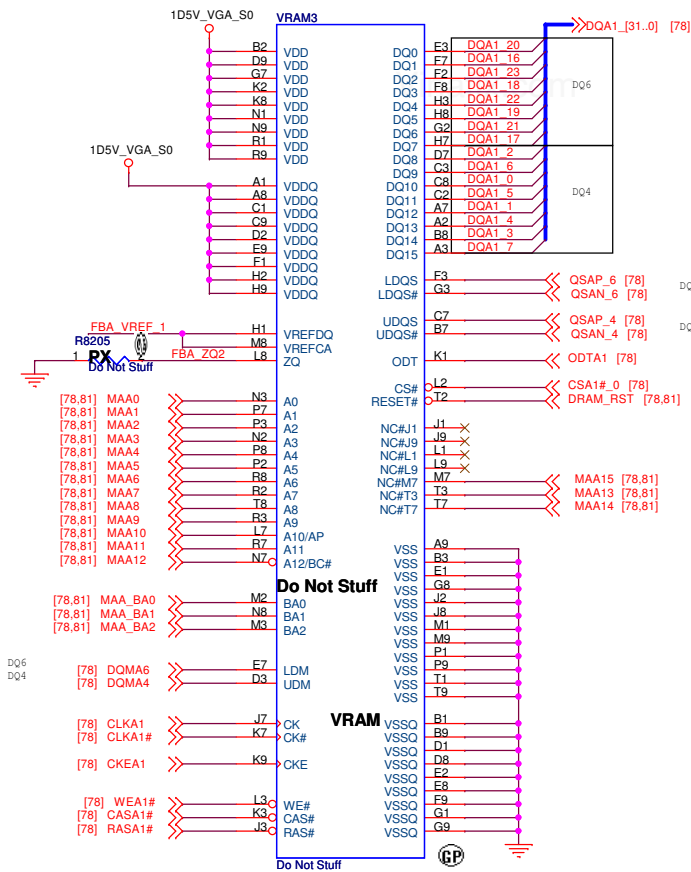


Frame Buffer Patition A-Lower Half

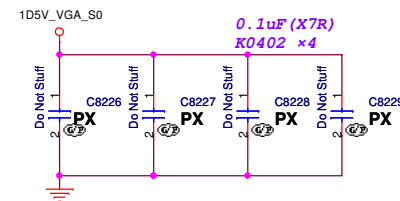


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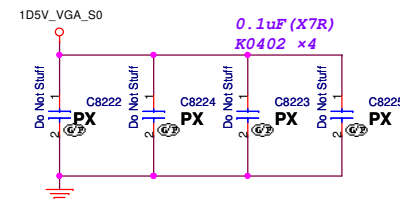
Main Func = Vram (DDR3L)



Place close VRAM3VDDQ ball

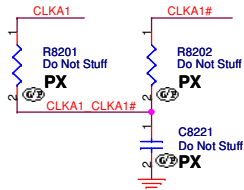


Place close VRAM4VDDQ ball

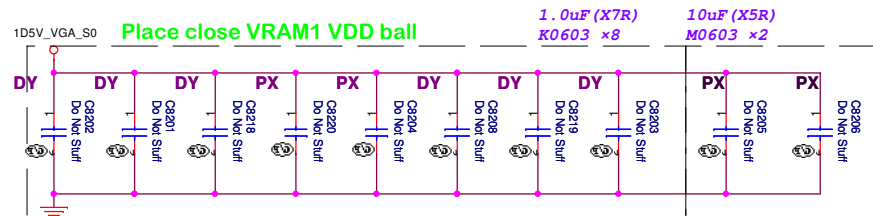
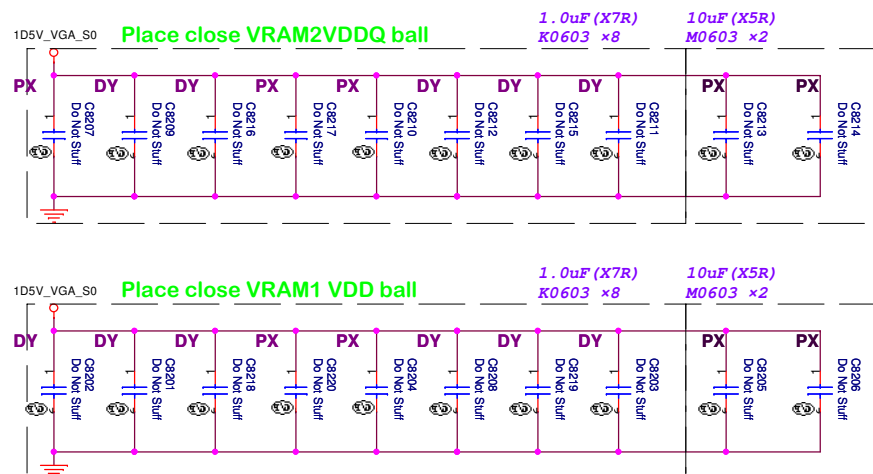
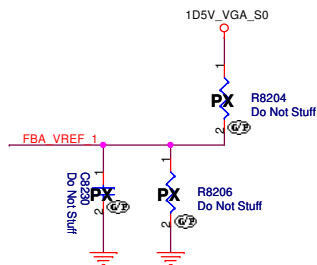


R7905 R7910

Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



Frame Buffer Patition A-Lower Half



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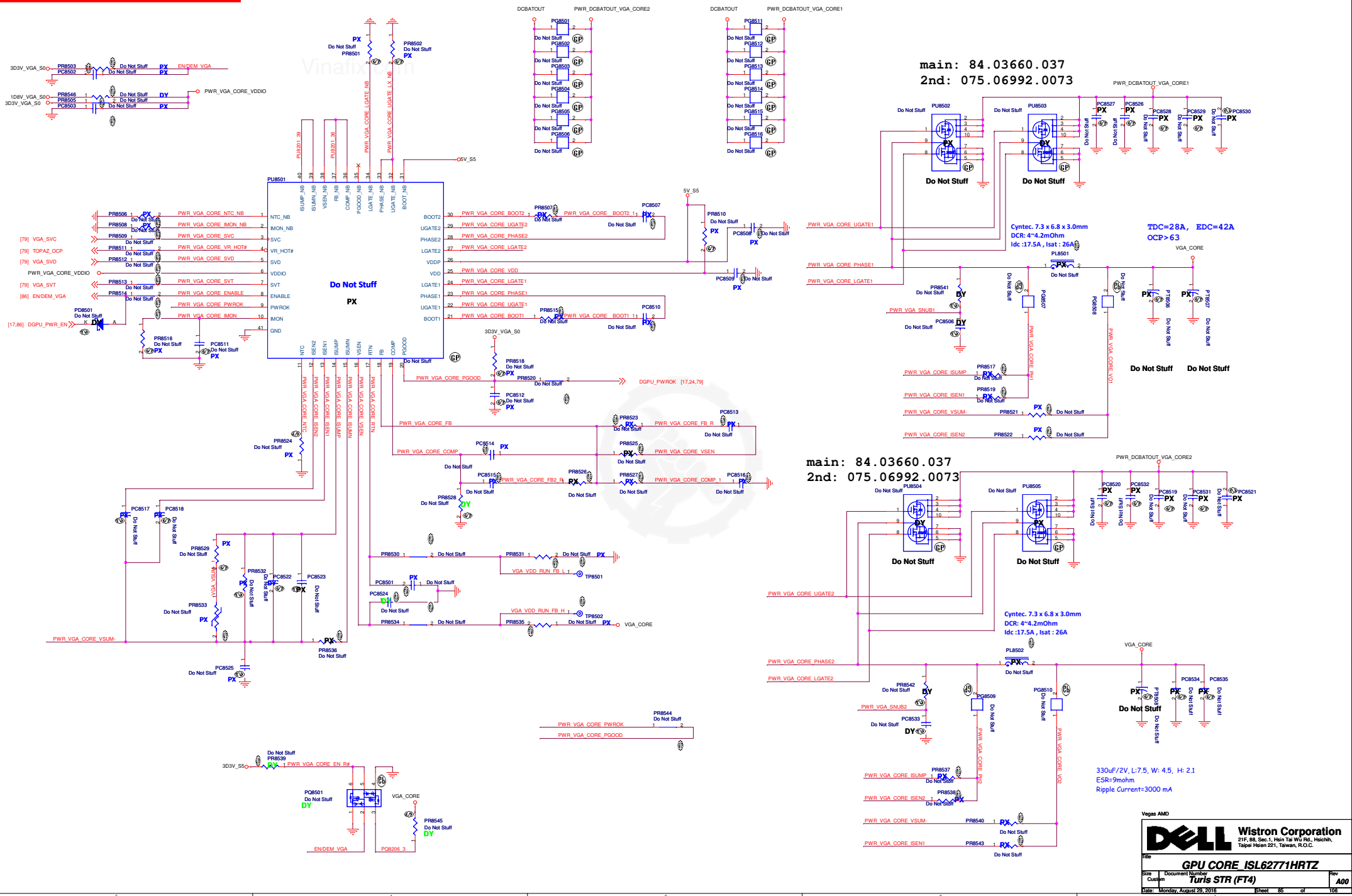
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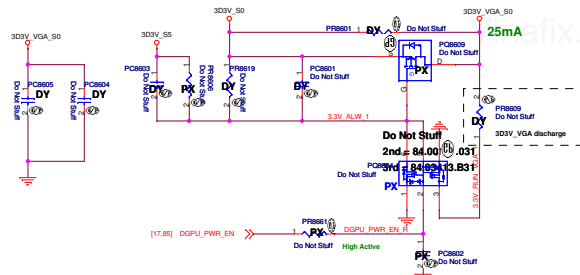
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Main Func = dGPU power



3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D35V_VGA_S0

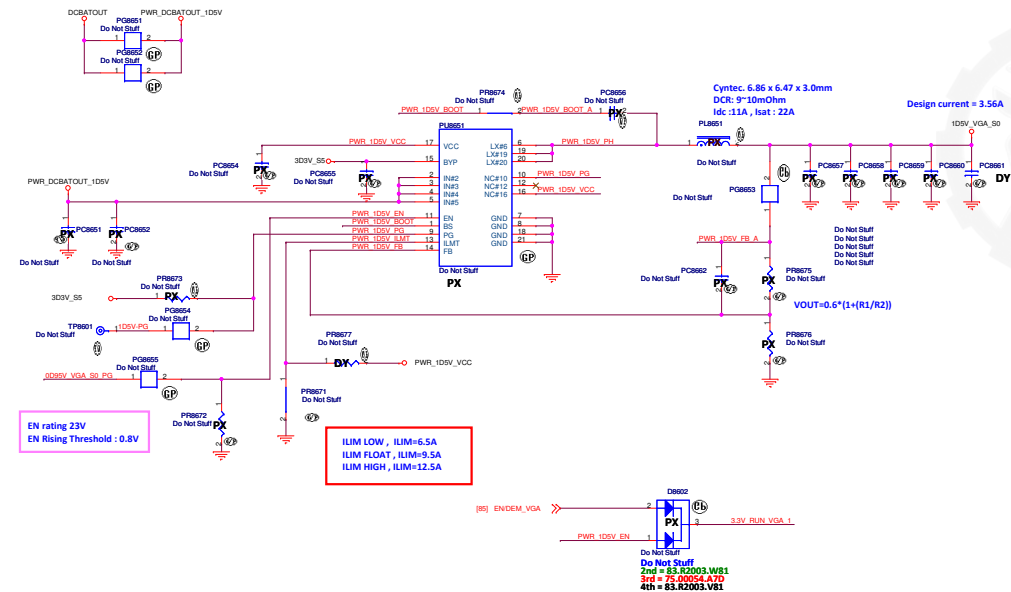
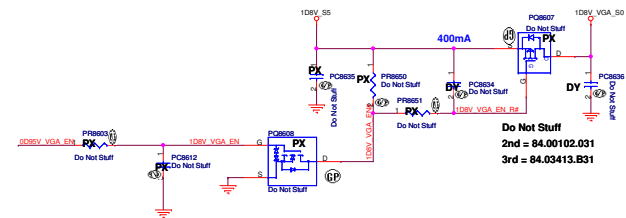
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages within **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

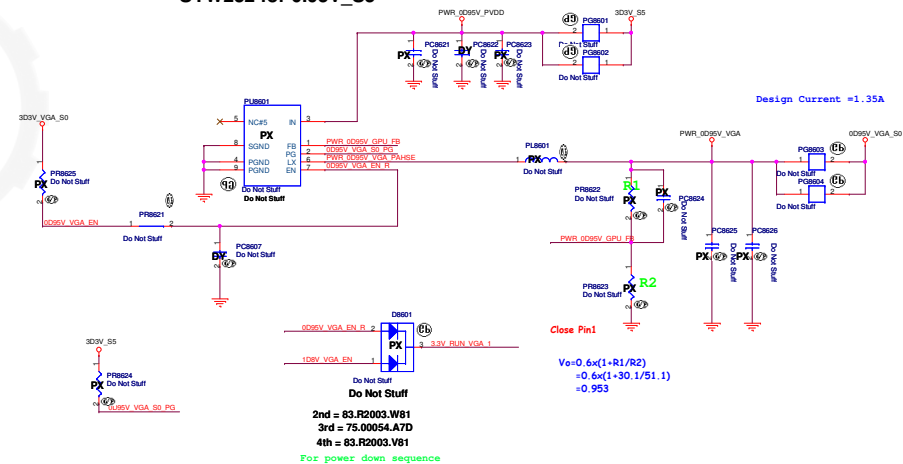
It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

1D8V_VGA_S0



SYW232 for 0.95V_S5





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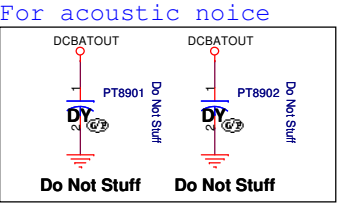
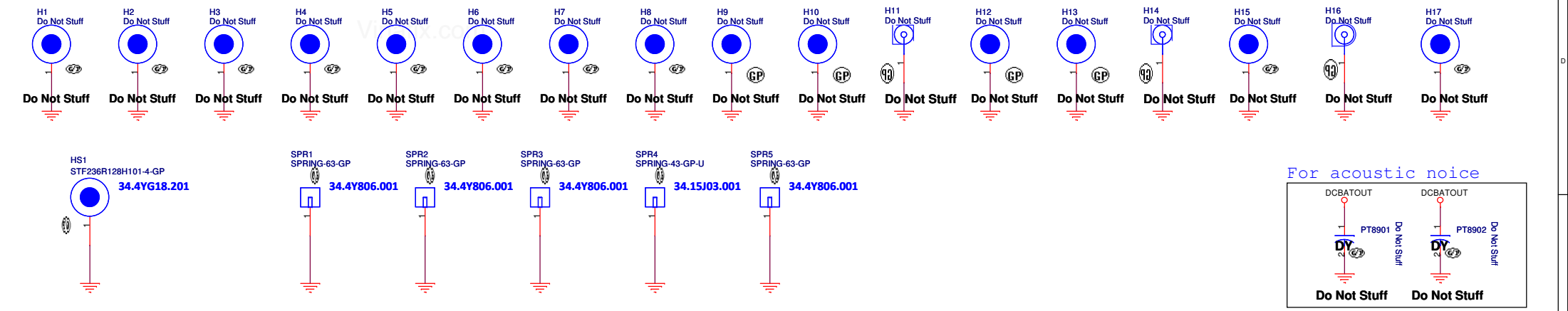
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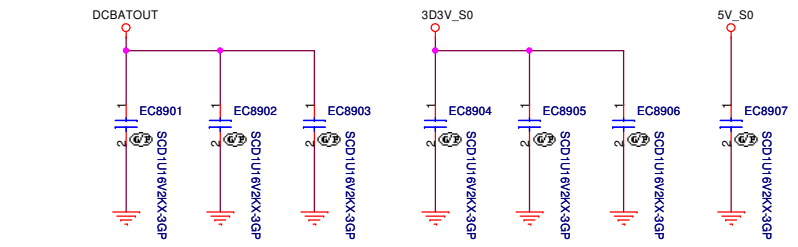
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Main Func = UnusedParts



Main Func = EMICapacitors



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004_ (Reserved)	040_Power Plane Enable&Sequence	076_GPU (1/5) PEG
005_CPU (DDR)	041_ (Reserved)	077_GPU (2/5) DIGITALOUT
006_ (Reserved)	042_DCIN JACK	078_GPU (3/5) VRAM I/F
007_CPU (VCC_CORE)	043_BATT CONN	079_GPU (4/5) GPIO/STRAP
008_CPU (DISPLAY/SVI2/JTAG/TES)	044_CHARGER ISL88739	080_GPU (5/5) PWR/GND
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010_CPU (Power CAP1)	046_ISL62771_CPUCORE (1/2)	082_VRAM3,4 (2/2)
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012_DDR4-SODIMM1	048_ (Reserved)	084_ (Reserved)
013_DDR4-SODIMM2	049_VDDCRGFX_APL5337	085_GPU CORE ISL62771HRTZ
014_ (Reserved)	050_ (Reserved)	086_DISCRETE VGAPOWER
015_ (Reserved)	051_ (Reserved)	087_ (Reserved)
016_CPU (CLK/SATA/USB/SPI/LPC)	052_APW8861_OD95V	088_ (Reserved)
017_CPU (ACPI/SD/AZ/GPIO/RTC)	053_VDDQ&VTT&VPP_APW8861	089_UNUSED PARTS/EMI Capacitors
018_ (Reserved)	054_DC2DC_1D8V/1D5V	090_ (Reserved)
019_ (Reserved)	055_LCD/Inverter CONN	091_ (Reserved)
020_CPU Strappings	056_VGA	092_ (Reserved)
021_ (Reserved)	057_HDMI	093_ (Reserved)
022_ (Reserved)	058_ (Reserved)	094_ (Reserved)
023_ (Reserved)	059_ (Reserved)	095_ (Reserved)
024_KBC Nuvoton NPCE985	060_SATA IF HDD/ODD	096_ (Reserved)
025_Flash (KBC+PCH) /RTC	061_NGFF_WLAN CONN	097_ (Reserved)
026_THERMAL NCT7718W/Fan	062_ (Reserved)	098_ (Reserved)
027_Audio Codec ALC3234	063_ (Reserved)	099_ (Reserved)
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033_ (Reserved)	069_ (Reserved)	105_SMBUS BLOCK DIAGRAM
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035_USB Power SW	071_ (Reserved)	
036_USB PORT1~3	072_ (Reserved)	

Change notes

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Title	Author	Year	Source
1. The Role of the Teacher in the 21st Century	John Hattie	2009	Visible Learning
2. The Science of Learning: How the Brain Works	David Sousa	2006	Corwin Press
3. The Power of Learning Styles	Richard Felder and Linda Soler	2005	John Wiley & Sons
4. The Art of Teaching: A Practical Guide	Robert G. Mager	1978	Harvard University Press
5. The Teacher's Guide to the 21st Century	Michael Fullan	2007	Corwin Press
6. The Science of Learning: How the Brain Works	David Sousa	2006	Corwin Press
7. The Power of Learning Styles	Richard Felder and Linda Soler	2005	John Wiley & Sons
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9. The Teacher's Guide to the 21st Century	Michael Fullan	2007	Corwin Press
10. The Science of Learning: How the Brain Works	David Sousa	2006	Corwin Press

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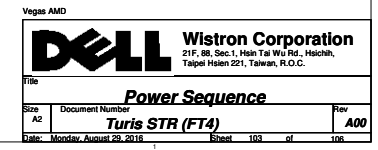
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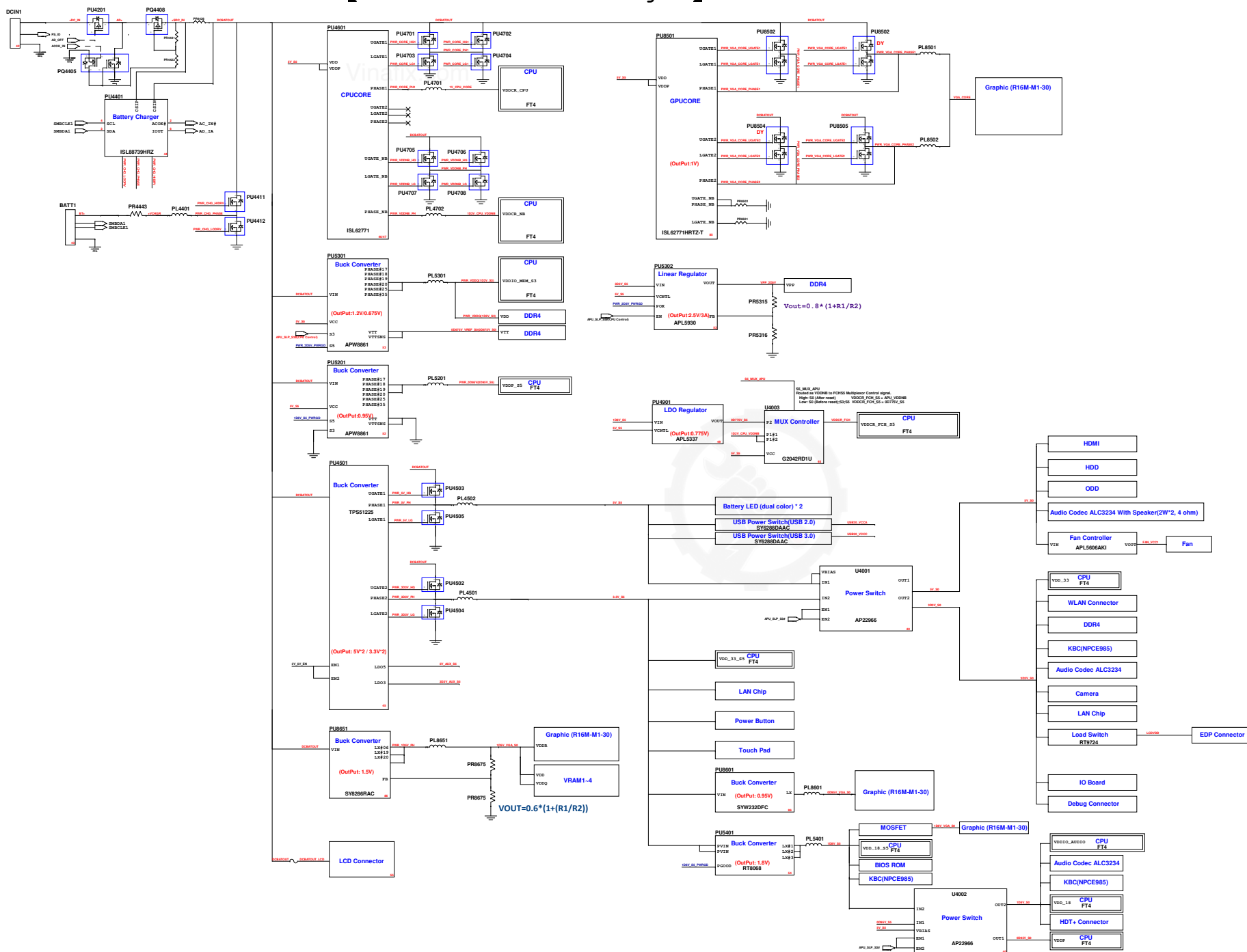
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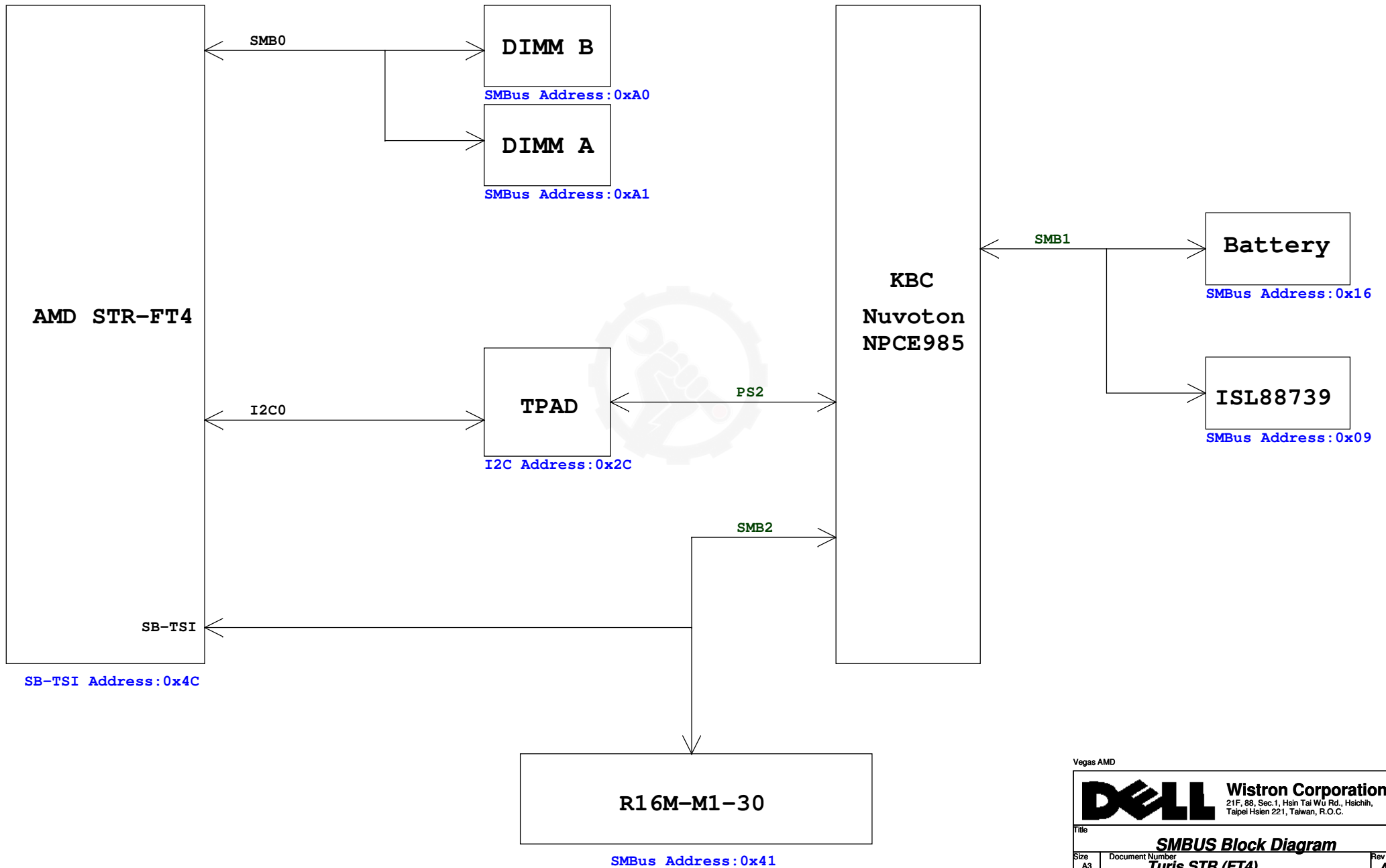
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【Turis AMD Power Block Diagram】

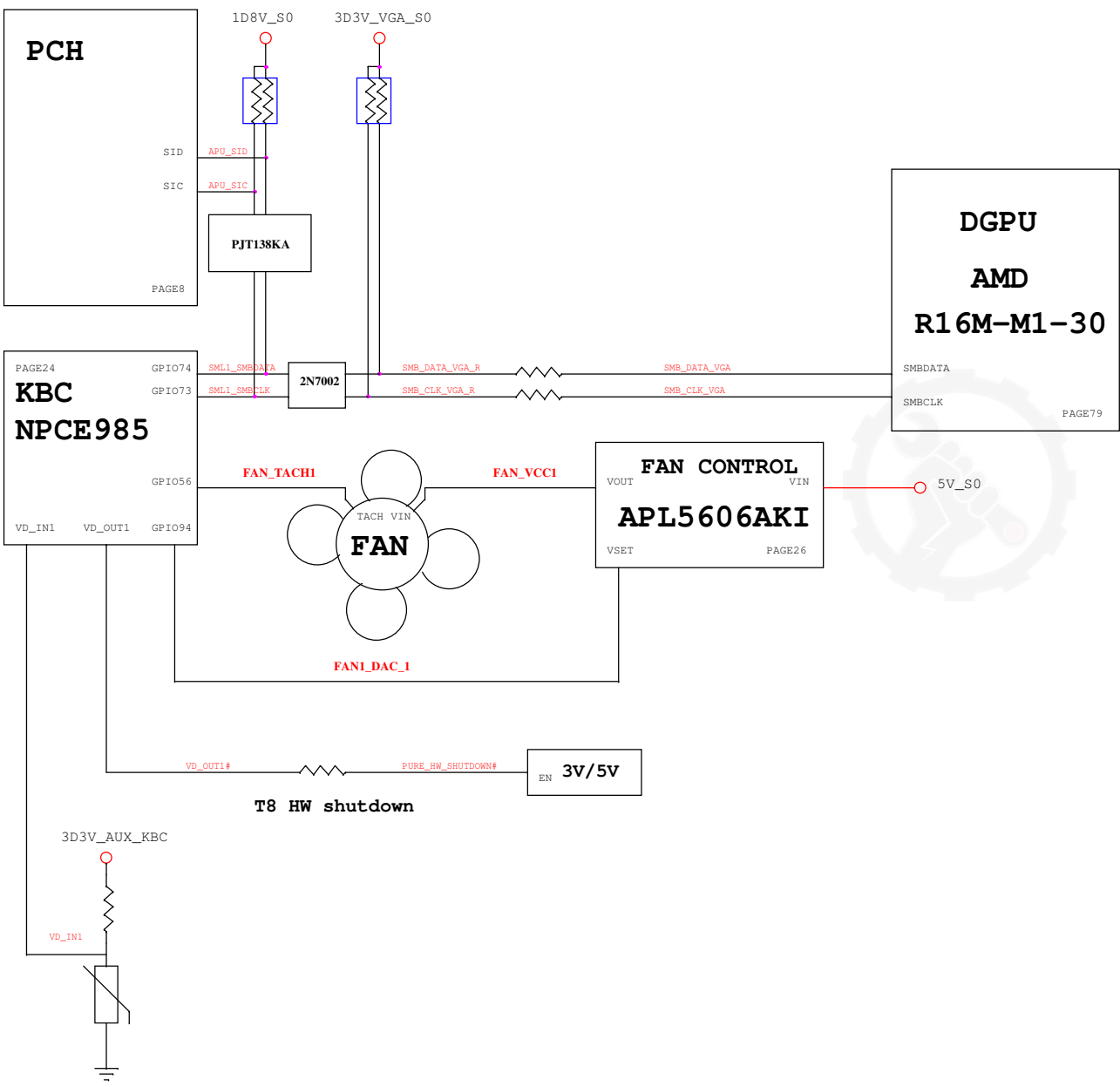




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Thermal Block Diagram

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Audio Block Diagram

